

# Circuits from the Lab Reference Designs

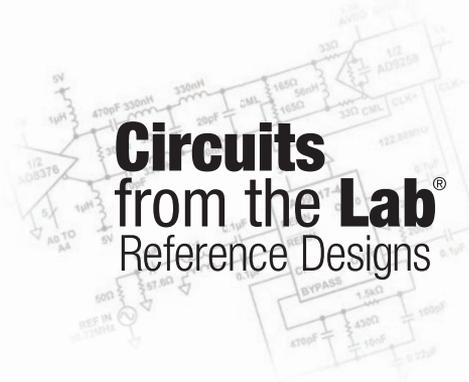
## Precision Data Acquisition

### About Circuits from the Lab Reference Designs

ADI Circuits from the Lab® Reference Designs are built and tested for function and performance by ADI's applications experts. Circuits from the Lab support quick and easy evaluation, prototyping, and design integration, and offer:

- Comprehensive documentation
- Complete design and integration files
- Factory tested evaluation hardware

Precision Data Acquisition Circuits from the Lab Reference Designs are application agnostic and are commonly used in analog signal chain design as standalone solutions, or to build more complex circuits and subsystems.



### Precision Data Acquisition

#### Application Introduction

Precision data acquisition systems (DAQs) are essential to many medical, industrial, instrumentation, and military applications. Resolution requirements range from 16 bits to 24 bits, and sampling rates from a few Hz to several MHz. In multichannel systems, analog multiplexers allow a single analog-to-digital converter (ADC) to sample a number of channels, thereby lowering cost and printed circuit board real estate. Choosing the proper ADC is an important design consideration, as well as the supporting circuitry, including the voltage reference, input drive amplifier, instrumentation amplifier, multiplexer, and power supply.

#### Design Considerations and Major Challenges

Successive approximation (SAR) and sigma-delta ( $\Sigma$ - $\Delta$ ) are the most popular ADC architectures for data acquisition systems. However, choosing the correct architecture for an application can be a challenging task. Successive approximation ADCs are available with resolutions of up to 18 bits and sampling rates of several MSPS (see [CN0277](#) that highlights the [AD7960](#) 18-bit, 5 MSPS ADC). They are ideal for multiplexed applications requiring a large number of channels (see [CN0254](#) and [CN0269](#)). SAR ADCs find widespread applications in medical imaging, electronic test and measurement, and industrial applications such as programmable logic controllers (PLCs) and distributed control systems (DCSs).

$\Sigma$ - $\Delta$  ADCs have resolutions up to 24 bits and are ideal for precision measurement applications that use low sampling rates (see [CN0251](#) and [CN0310](#)). High resolution allows a direct interface to many sensors such as thermocouples, load cells, and RTDs. Some  $\Sigma$ - $\Delta$  ADCs have internal programmable gain amplifiers that facilitate processing low level signals without the requirement for additional gain components.

The design of a DAQ can be quite challenging because of the many trade-offs possible. For example, industrial signals of  $\pm 10$  V require special conditioning to interface with single-supply differential input ADCs (see [CN0251](#), [CN0269](#), and [CN0310](#)). Harsh industrial environments may also require high voltage digital isolators to protect sensitive circuits (see [CN0254](#)). Making the proper trade-offs between power dissipation, dynamic performance, PCB area, and cost is important for a competitive design, and achieving required performance depends on careful attention to layout, grounding, and decoupling techniques.



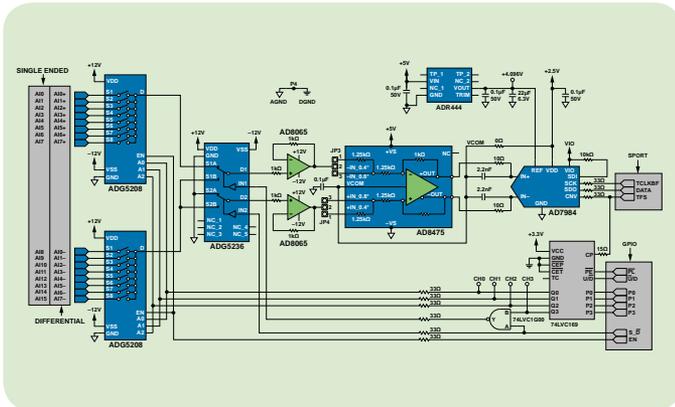
## Circuits from the Lab Reference Designs—Precision Data Acquisition

Circuits from the Lab Reference Designs	Resolution (Bits)	Sampling Rate (kSPS)	Number of Channels	Converter Architecture	Input Signal Range (V)	Power Dissipation (mW)	Data Output Format	Additional Features	Evaluation Hardware	Pricing (\$/ea)
CN0310	24	250	1	$\Sigma$ - $\Delta$	$\pm 10$ , $\pm 5$ , 0 to +10	54	SPI		EVAL-AD7176-2SDZ*	59.00
CN0251	24	4.7 Hz	4	$\Sigma$ - $\Delta$	$\pm 10$ , $\pm 5$ , $\pm 1$ , $\pm 500$ mV, $\pm 250$ mV, $\pm 125$ mV, $\pm 62$ , 5 mV, $\pm 31.25$ mV	130	SPI		EVAL-CN0251-SDPZ*	80.00
CN0277	18	5 MSPS	1	PuISAR®	0 to +5	122	LVDS	Optimized for ac performance	EVAL-AD7960FMCZ**	99.00
CN0269	18	1.33 MSPS	16	PuISAR	$\pm 10$ , $\pm 5$	337	SPI		EVAL-CN0269-SDPZ*	100.00
CN0261	18	250	1	PuISAR	0 to +5	107	SPI	Optimized for ac performance	EVAL-CN0261-SDPZ*	79.00
CN0305	16	300	1	PuISAR	0 to +5	11	SPI	Optimized for sub-Nyquist input signals up to 4 kHz	EVAL-CN0305-SDPZ*	99.00
CN0254	16	250	8	PuISAR	$\pm 10$	294	SPI	Isolated	EVAL-CN0254-SDPZ*	75.00
CN0306	16	100	1	PuISAR	0 to +5	7.4	SPI		EVAL-CN0306-SDPZ*	99.00
CN0255	16	100	1	PuISAR	0 to +2.5	8	SPI	Optimized for sub-Nyquist input signals up to 4 kHz	EVAL-CN0255-SDPZ*	79.00

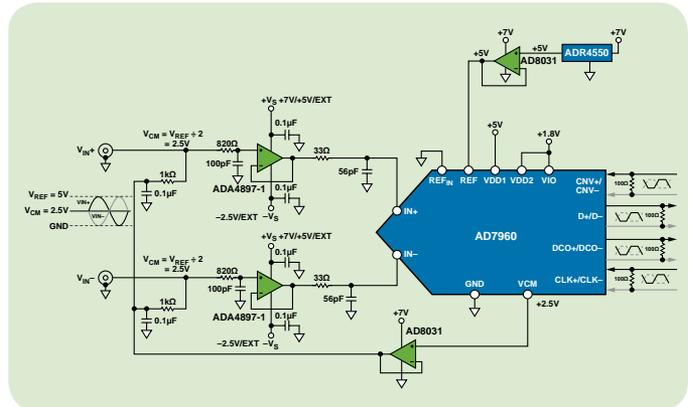
\* This reference design also requires EVAL-SDP-CB1Z (\$99.00)

\*\* This reference design also requires EVAL-SDP-CH1Z (\$199.00)

## Highlighted Circuits from the Lab Reference Designs



CN0269: 18-bit, 1.33 MSPS, 16-channel data acquisition system.



CN0277: high precision, 18-bit, 5 MSPS, low power data acquisition signal chain.

## Key Products

### Analog-to-Digital Converters

Part Number	Resolution (Bits)	Throughput Rate Max (kSPS)	Architecture	Full Power BW (MHz)	Number of Channels	Package
AD7176-2	24	250	$\Sigma$ - $\Delta$	N/A	4	TSSOP
AD7192	24	4.8	$\Sigma$ - $\Delta$	N/A	4	TSSOP
AD7960	18	5 MSPS	PuISAR	28	1	LFCSP
AD7691	18	250	PuISAR	2	1	MSOP, LFCSP
AD7984	18	1.33 MSPS	PuISAR	10	1	MSOP, LFCSP
AD7689	16	250	PuISAR	1.7	8	LFCSP
AD7988-5	16	500	PuISAR	10	1	MSOP, LFCSP
AD7988-1	16	100	PuISAR	10	1	MSOP, LFCSP

### Rail-to-Rail Output Fully Differential Funnel Amplifier

Part Number	-3 dB BW (MHz)	Slew Rate (V/ $\mu$ s)	Closed-Loop Gain	Input Offset Voltage ( $\mu$ V)	Min Pos Supply (V)	Max Pos Supply (V)	Supply Current per Amplifier (mA)	Amplifiers per Package	Package
AD8475	150	50	0.4, 0.8	200	3	10	3	1	MSOP, LFCSP

### Rail-to-Rail Output Instrumentation Amplifier

Part Number	Gain (Min)	Gain (Max)	Min CMRR @ 60 Hz, G = 1 (dB)	V <sub>SUPPLY</sub> Span Min (V)	V <sub>SUPPLY</sub> Span Max (V)	Supply Current ( $\mu$ A)	Voltage Noise RTI ( $\mu$ V p-p)	Package
AD8226	1	1000	86	2.2	36	400	2	MSOP, SOIC

### Operational Amplifiers

Part Number	Small Signal Bandwidth (MHz)	Slew Rate (V/ $\mu$ s)	Input Offset Voltage ( $\mu$ V)	Amplifiers per Package	V <sub>SUPPLY</sub> Span Min (V)	V <sub>SUPPLY</sub> Span Max (V)	Rail-Rail Input/Output	Supply Current per Amplifier (mA)	Package
AD8031	80	35	1 mV	1	2.7	12	Input, output	0.9	PDIP, SOIC, SOT-23
AD8032	80	35	1 mV	2	2.7	12	Input, output	0.9	PDIP, SOIC, MSOP
ADA4897-1	230	120	28	1	3	10	Output	3	SOIC, SOT-23
ADA4897-2	230	120	28	2	3	10	Output	3	MSOP
AD8065	145	180	400	1	5	24	Output	6.4	MSOP, SOIC, SOT-23
AD8597	10	14	10	1	10	36		4.8	SOIC, LFCSP
OP1177	1.3	0.7	15	1	5	36		0.4	MSOP, SOIC
AD8605	10	5	20	1	2.7	6	Input, output	1	SOT-23, WLCSP
AD8608	10	5	20	4	2.7	6	Input, output	1	SOIC, TSSOP
AD8609	400 kHz	0.1	12	4	1.8	5	Input, output	0.05	SOIC, TSSOP
AD8641	3.5	3	50	1	5	26	Output	0.25	SC70, SOIC
ADA4841-1	80	13	40	1	2.7	12	Output	1.1	SOT-23, SOIC

### Voltage References

Part Number	V <sub>OUT</sub> (V)	Initial Accuracy (%)	Ref Out TC (ppm/ $^{\circ}$ C)	0.1 Hz to 10 Hz Noise ( $\mu$ V p-p)	Reference Type	Max Input Voltage (V)	Dropout Voltage (mV)	Package
ADR445	5	0.04	1	2.25	Series low dropout	18	500	MSOP, SOIC
ADR444	4.096	0.04	1	1.8	Series low dropout	18	500	MSOP, SOIC
ADR4550	5	0.02	2	2.8	Series low dropout	15	300	SOIC
ADR435	5	0.04	1	8	Series	18	2 V	MSOP, SOIC
ADR4525	2.5	0.02	2	1.25	Series low dropout	15	300	SOIC

### isoPower Digital Isolators

Part Number	Number of Inputs Side 1	Number of Inputs Side 2	Insulation Rating (kV rms)	Max Data Rate (Mbps)	Prop Delay (ns)	Isolated Output Supply (mA)	Isolated Output Voltage Min/Max (V)	Max Pos Supply (V)	Package
ADuM3471	3	1	2.5	25	60	400	3.3/24	5.5	SSOP

## Linear Regulators

Part Number	V <sub>IN</sub> Min (V)	V <sub>IN</sub> Max (V)	V <sub>OUT</sub> Preset	Max V <sub>OUT</sub> Adj (V)	Min V <sub>OUT</sub> Adj (V)	I <sub>OUT</sub> (Max) (mA)	Dropout Voltage @ Rated I <sub>OUT</sub> (mV)	Package
ADP1720	4	28	3.3, 5.0	5	1.225	50	275	MSOP
ADP3336	2.6	12	N/A	10	1.5	500	200	MSOP

## Analog Multiplexers

Part Number	Sw/Mx Function × Number	Max Analog Signal Range	-3 dB Bandwidth (MHz)	Supply V Guar Performance (V)	R <sub>ON</sub> (Ω)	Transistion Time (ns)	Package
ADG5208	(8:1) × 1	V <sub>SS</sub> to V <sub>DD</sub>	54	Dual: (±15), Dual: (±20), Single: (+12), Single: (+36)	160	170	TSSOP, LFCSP
ADG5236	(2:1) × 2	V <sub>SS</sub> to V <sub>DD</sub>	266	Dual: (±15), Dual: (±20), Single: (+12), Single: (+36)	160	150	TSSOP, LFCSP
ADG1409	(4:1) × 2	V <sub>SS</sub> to V <sub>DD</sub>	115	Dual: (±15), Dual: (±5), Single: (+12)	4	140	TSSOP, LFCSP

## Additional Design Resources

### Technical Books and Articles

Data Conversion Handbook—[www.analog.com/library/analogdialogue/archives/39-06/data\\_conversion\\_handbook.html](http://www.analog.com/library/analogdialogue/archives/39-06/data_conversion_handbook.html)

- ADC Architectures (Chapter 3.2)
- Interfacing to Data Converters (Chapter 6)
- Multichannel Data Acquisition Systems (Chapter 8.2)

Which ADC Architecture Is Right for Your Application?, *Analog Dialogue*—[www.analog.com/library/analogdialogue/archives/39-06/architecture.html](http://www.analog.com/library/analogdialogue/archives/39-06/architecture.html)

A Practical Guide to High-Speed Printed-Circuit-Board Layout, *Analog Dialogue*—[www.analog.com/library/analogdialogue/archives/39-09/layout.html](http://www.analog.com/library/analogdialogue/archives/39-09/layout.html)

### Tutorials

- MT-021: Successive Approximation ADCs—[www.analog.com/MT-021](http://www.analog.com/MT-021)
- MT-022: Σ-Δ ADCs—[www.analog.com/MT-022](http://www.analog.com/MT-022)
- MT-031: Grounding Data Converters—[www.analog.com/MT-031](http://www.analog.com/MT-031)
- MT-101: Decoupling Techniques—[www.analog.com/MT-101](http://www.analog.com/MT-101)

### Design Tools and Forums

- Signal Chain Designer™ Advanced Selection and Design Environment—[www.analog.com/signalchaindesigner](http://www.analog.com/signalchaindesigner)
- EngineerZone™ Online Technical Support Community—[ez.analog.com](http://ez.analog.com)
- ADIsimADC™ Converter Modeling Tool—[www.analog.com/adisimadc](http://www.analog.com/adisimadc)

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