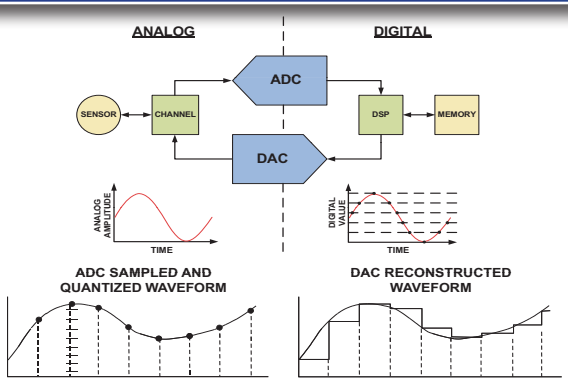
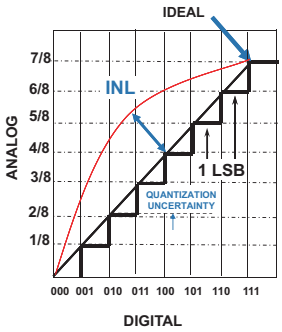
THE ESSENTIAL GUIDE TO DATA CONVERSION

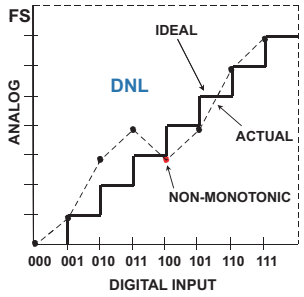
"Real-World" Sampled Data Systems Consist of ADCs and DACs



- Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) allow DSPs to interact with real-world signals.
- Real-world signals are continuous (analog) signals.
  - Pressure sensor
  - Temperature sensor, etc.
- Real-world signal processing allows for efficient and cost effective extraction of information from a signal.
  - Signal amplitude
  - Phase, etc.
- Digital information differs from real-world information in two important respects…it is sampled, and it is quantized. Both of these restrict how much information a digital signal can contain.

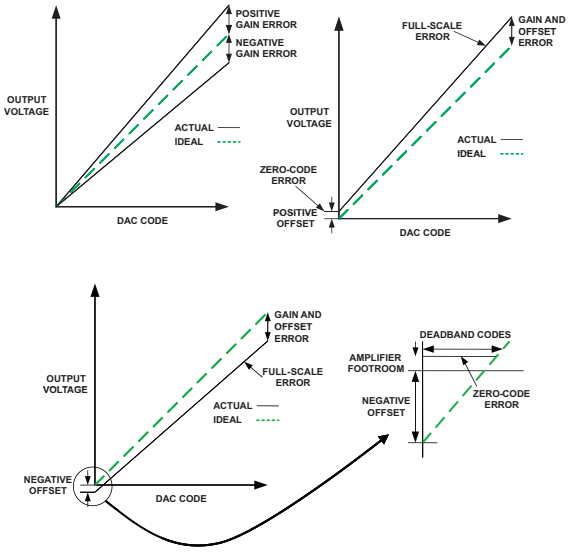
Converter Resolution, INL, and DNL





- Converter resolution represents the analog signal at a number of discrete levels or steps.
  - The smallest resolvable signal is 1 Least Significant Bit (LSB), which is equal to FS/8 in this example.
- Integral Nonlinearity (INL) is a measure of the maximum deviation in LSBs, from a straight line passing through negative full-scale and positive full-scale.
  - Good INL is required for open-loop systems and many closed-loop systems.
- Differential Nonlinearity (DNL) is the difference between the actual step size and the ideal 1 LSB change between two adjacent codes.
  - DNL error results in:
    - Smaller or larger step sizes than the ideal
    - Additive noise/spurs beyond the effects of quantization
- A DAC is monotonic if its output increases or remains the same for an increment in the digital code, i.e., DNL > –1 LSB (a key requirement in a control system).
  - Conversely, a DAC is nonmonotonic if the output decreases for an increment in the digital code.
- An ADC has no missing codes if the input voltage is swept over the entire input range and all output code combinations appear at the converter output. A DNL error of > –0.99 LSB guarantees that the converter will have no missing codes.

Converter Errors (Unipolar)



DAC Definitions

- Zero-Code Error is the measured output voltage from VOUT of the DAC when zero code (all zeros) is loaded to the DAC register.
  - Zero-Code Error is typically expressed in LSBs.
- DAC Offset Error is a measure of the difference between the actual VOUT and the ideal VOUT in the linear region of the transfer function. Offset error can be negative or positive in the DAC and output amplifier.
  - Offset Error is typically expressed in mV or mA.
- DAC Gain Error is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal.
  - Gain Error is usually expressed as a percentage of the full-scale range.
- Full-Scale Error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{REF} – 1 LSB. (Full-Scale Error = Offset Error + Gain Error)
  - Full-Scale Error is typically expressed as a percentage of the full-scale range.
- Deadband Errors, DACs with integrated output amplifiers will have performance degradation, deadbands, at codes outside of the linear region of the output amplifier.
  - The number of deadband codes depends on the DAC output voltage span, the headroom and footroom of the amplifier, and the power supply rails used.

ADC Definitions

- ADC Offset Error is the deviation of the first code transition, for example (000…000) to (000…001) from the ideal (A_{GND} + 1 LSB). Offset error is typically expressed in LSBs.
- ADC Gain Error is the deviation of the last code transition, for example (111…110) to (111…111) from the ideal (V_{REF} – 1 LSB) after the offset error is adjusted out. Gain error for an ADC does not include the reference error and is typically expressed in LSBs.

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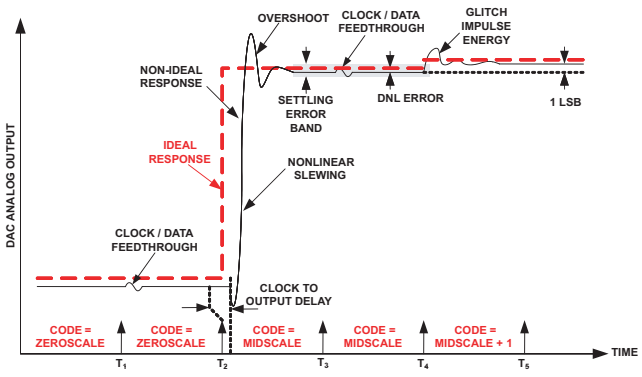
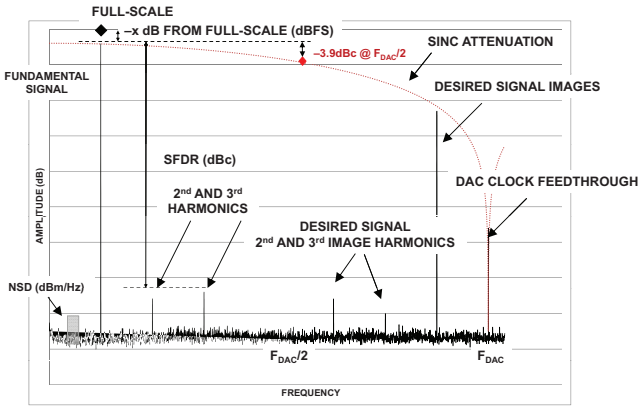
Time Domain DAC Output



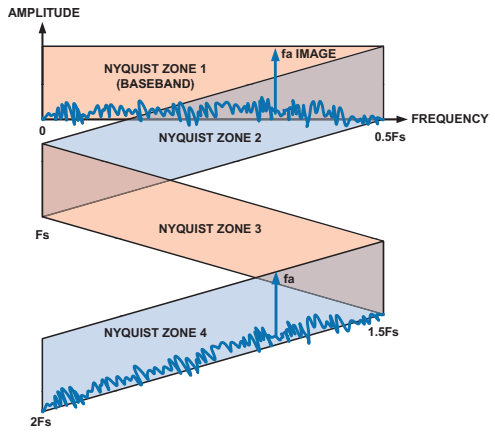
- **Clock to output delay**
  - Group delay due to DAC propagation delay
- **Settling time**
  - Measured relative to output signal alone
  - Time between when signal leaves ±0.5 LSB error band to when it remains within ±0.5 LSB error band of final value
- **Slew rate**
  - Defined as maximum rate of change of voltage or current at output
  - Specified as V/sec or A/sec depending on DAC output stage
  - Typically measured for full-scale step size with 10% to 90% error band
- **Glitch impulse energy**
  - Caused by unequal propagation delays within DAC
  - Often measured for midscale LSB transition (011..111 to 100..000)
  - Measured as "area" of glitch impulse with units p/nV-s or p/nA-s

Frequency Domain DAC Output



- **Sinc(x)**
  - DAC's time domain step response (zero-order hold) modifies DAC frequency response
  - DAC output signals are attenuated by $\sin(\pi f/f_{dac})/(\pi f/f_{dac})$ envelope
- **Harmonics**
  - Created by DAC's static and dynamic nonlinearities
- **Images**
  - Duplicate of the desired signal (and its DAC induced harmonics) at higher Nyquist zones
  - Images are predicted by sampling theory
- **SFDR**
  - Measured with single-tone output in first Nyquist band (unit is dBc)
  - Difference between single-tone amplitude to the next highest spurious tone
- **Noise Spectral Density (NSD)**
  - Integration of the noise floor in a small frequency band (unit is dBm/Hz or nV/rtHz)

Nyquist's Criteria



- Undersampled analog signal f_a sampled @ F_s has images (aliases) at $|\pm KF_s \pm f_a|$, K = 0.5, 1, 1.5 …
- A signal with a maximum frequency f_a must be sampled at a rate $F_s > 2f_a$ or information about the signal will be lost because of aliasing.
- Aliasing occurs whenever $F_s < 2f_a$.
- The concept of aliasing is widely used in communications applications such as direct IF-to-digital conversion.
- A signal that has frequency components between f_a and f_b must be sampled at a rate $F_s > 2 (f_b – f_a)$ in order to prevent alias components from overlapping the signal frequencies.

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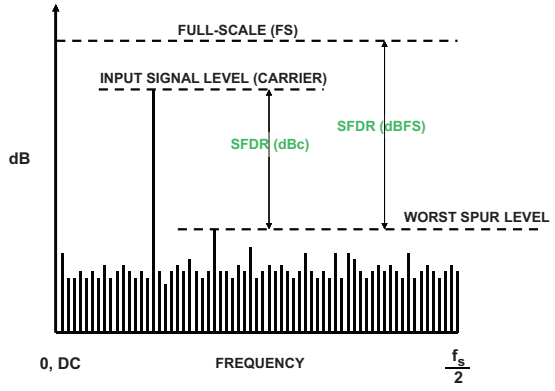
Analog-to-Digital Converter AC Performance Specifications



- **SNR (Signal-to-Noise Ratio, dB or dBFS)**
  - The ratio of the RMS value of the measured output signal (peak or full scale) to the RMS sum of all other spectral components excluding the first 6 harmonics and DC.

  RMS Signal = (FSR / 2) / √(2), RMS Noise = Qn = q / √(12)

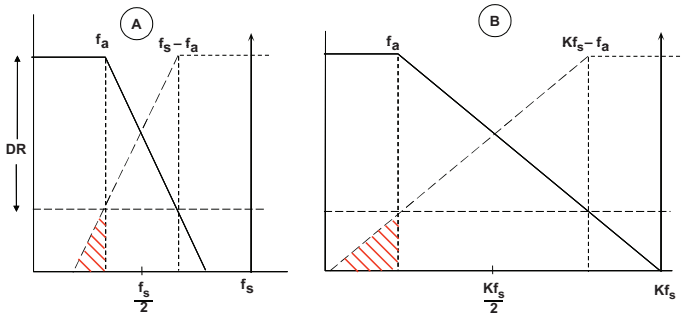
  SNR (dB) = RMS Signal / RMS Noise = $20 \times \log(2^{(n-1)} \times \sqrt{6}) = 6.02 \times n + 1.76$
- **SINAD (Signal-to-Noise Ratio and Distortion, dB)**
  - The ratio of the RMS signal amplitude to the RMS value of the sum of all other spectral components including harmonics, but excluding DC.

  SINAD (dB) = $-20 \times \log(\sqrt{(10^{(-\text{SNR W/O DIST}/10)} + 10^{(\text{THD}/10)})})$

  ENOB (BITS) = (SINAD – 1.76 + 20 × log (FSR/Actual FSR)) / 6.02
- **THD (Total Harmonic Distortion, dB)**
  - The ratio of the RMS sum of the first 6 harmonics to the RMS value of the measured fundamental.

  THD (–dB) = $20 \times \log(\sqrt{(10^{(-2\text{ND HAR}/20)})^2 + (10^{(-3\text{RD HAR}/20)})^2 + \ldots (10^{(-6\text{TH HAR}/20)})^2})$
- **SFDR (Spurious-Free Dynamic Range, dB or dBFS)**
  - The ratio of the RMS value of the peak signal amplitude (or full-scale) to the RMS value of the amplitude of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Oversampling Relaxes Requirements on Baseband Antialiasing Filter

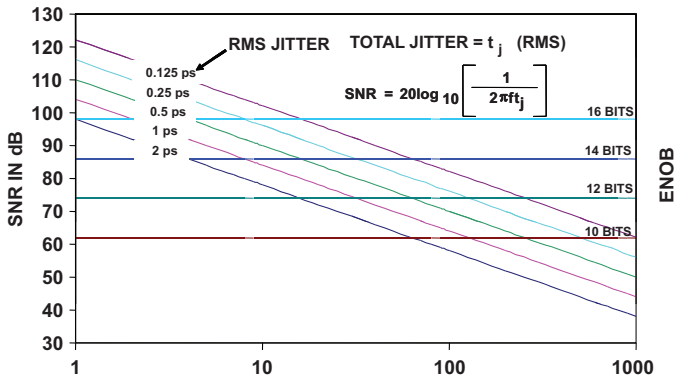


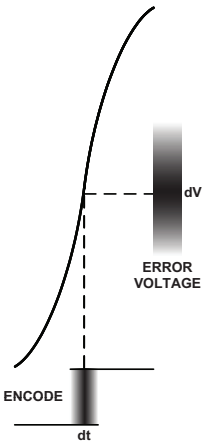
STOPBAND ATTENUATION = DR
TRANSITION BAND: f_a to $f_s - f_a$
CORNER FREQUENCY: f_a

STOPBAND ATTENUATION = DR
TRANSITION BAND: f_a to $Kf_s - f_a$
CORNER FREQUENCY: f_a

- **Generally an antialiasing filter is required on the analog front end of an ADC.**
  - If the sampling frequency is not much greater than the max input frequency f_a, then the requirements on an antialiasing filter can be severe, as in (A).
  - The dotted regions indicate where the dynamic range can be limited by signals outside the bandwidth of interest.
- **Oversampling relaxes the requirements of the analog antialiasing filter as shown in (B).**
  - Sigma-delta converters are a good example.
- **Outputs of DACs need filtering also, and these are called "anti-imaging" filters. They serve essentially the same purpose as the antialiasing filter ahead of an ADC.**

Theoretical SNR and ENOB Due to Jitter vs. Full-scale Sinewave Analog Input Frequency





- **The total amount of jitter is dependent on the effective aperture jitter within the converter, as well as the external jitter generated by the sampling clock circuit.**
  - These terms are root sum squared to determine the total amount of jitter applied to the signal chain.

TOTAL JITTER = $\sqrt{(\text{ADC APERTURE JITTER})^2 + (\text{SAMPLING CLOCK JITTER})^2}$

- **In this example, if a 12-bit ENOB, 74 dB SNR is desired for the design with an analog input frequency of 100 MHz, then the total jitter required must be 0.5 ps or less.**

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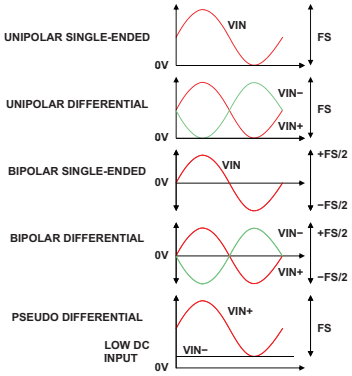
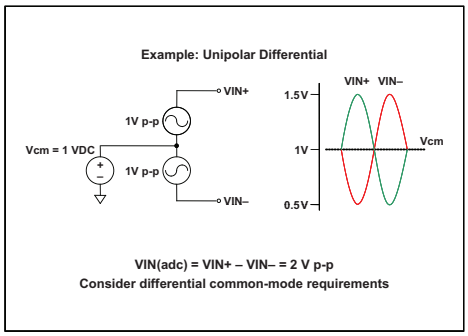
Analog Input/Output Configurations

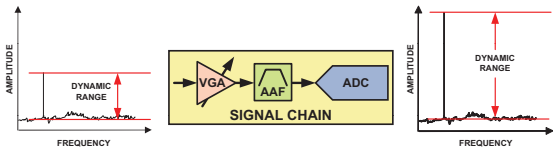




- Single-ended signaling is most common.
- Differential signals measure the difference in voltage between the positive and negative input terminals.
  - The inputs are 180 degrees out of phase with each other.
- Many benefits in using differential inputs.
  - Input transient reduction
  - Input noise reduction
  - Signal swing is doubled
- Pseudo differential is a single-ended/differential hybrid.
  - Separation of signal ground from ADC ground for the ADC conversion
- Consider ADC common-mode requirements Vcm = (Vp + Vn) / 2.
- The ADC converts VIN+ – VIN–.

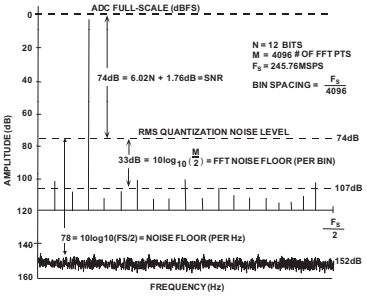
What Resolution Do I Need? Dynamic Range vs. Signal-to-Noise Ratio Requirements

- Dynamic Range (DR) is the difference in level between the highest signal peak that can be reproduced by the system and the amplitude of the highest spectral component of the noise floor.
  - DR provides amplitude range so the converter can "see" the signal of interest.
  - Converter DR is limited by SFDR and, theoretically, by its resolution.
- Consider using analog gain to increase DR capability of the system.



- Example: 10-bit ADC with an FSR = 4 V p-p has an LSB = 3.9 mV p-p or $4/2^{BITS}$. Therefore, 4 V / 3.9 mV = 1024 codes. This can also be expressed in dB or 20 × log (1024) = 60 dB.

- Signal-to-Noise Ratio (SNR) is the difference in level between the RMS signal level and the RMS level of the noise floor, except the first six harmonics and DC.
  - SNR limits the capability of the converter to see "small" signals.
  - Converter SNR is, theoretically, limited by its resolution.
  - Quantization noise of an ideal ADC will have an SNR = 6.02N + 1.76 (dB), N = Number of bits.
  - Effective Number of Bits (ENOB) is calculated from SNR: ENOB = (SNR – 1.76) / 6.02 (bits).



Quantization: The Size of a Least Significant Bit (LSB)

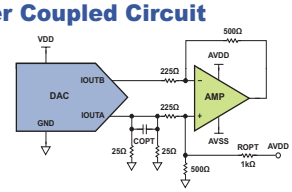
RESOLUTION N	2^N	VOLTAGE (2 V/10 V FS)	ppm FS	% FS	dBFS
2-bit	4	0.5/2.5 V	250,000	25	–12
4-bit	16	125/625 mV	62,500	6.25	–24
6-bit	64	31.3/156 mV	15,625	1.56	–36
8-bit	256	7.8/39.1 mV	3906	0.39	–48
10-bit	1024	2/9.77 mV	977	0.098	–60
12-bit	4096	0.49/2.44 mV	244	0.024	–72
14-bit	16,384	122/610 µV	61	0.0061	–84
16-bit	65,536	30.5/153 µV	15	0.0015	–96
18-bit	262,144	7.6/38 µV	4	0.0004	–108
20-bit	1,048,576	1.9/9.54 µV	1	0.0001	–120
22-bit	4,194,304	0.47/2.38 µV	0.24	0.000024	–132
24-bit	16,777,216	119/596 nV*	0.06	0.000006	–144

*600 nV is the Johnson Noise in a 10 kHz BW of a 2.2 kΩ resistor @ 25°C.

Remember: 10 bits and 10 V FS yields an LSB of 10 mV, 1000 ppm, or 0.1%. (All other values may be calculated by powers of 2.)

Converter Circuits

DAC Amplifier Coupled Circuit



ADC Amplifier Coupled Circuit