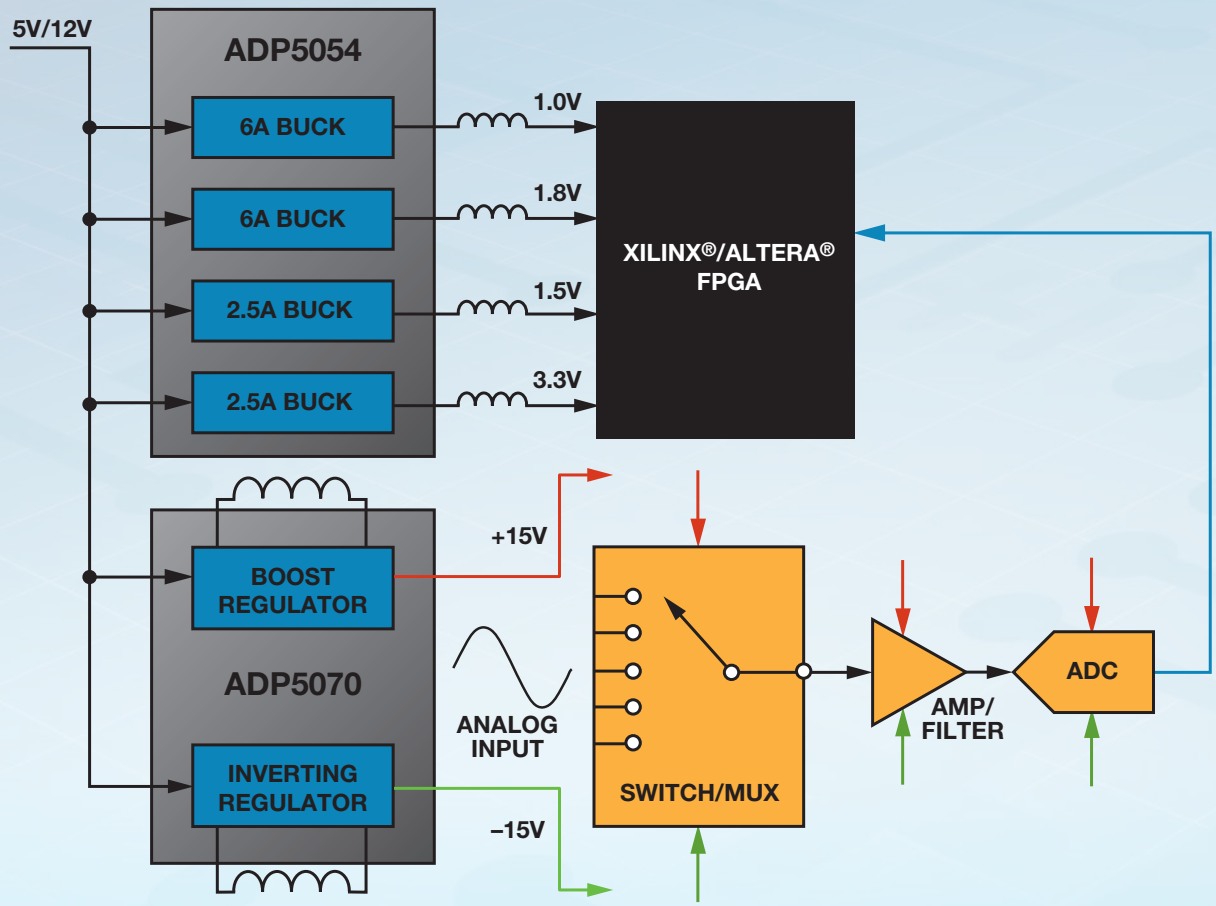
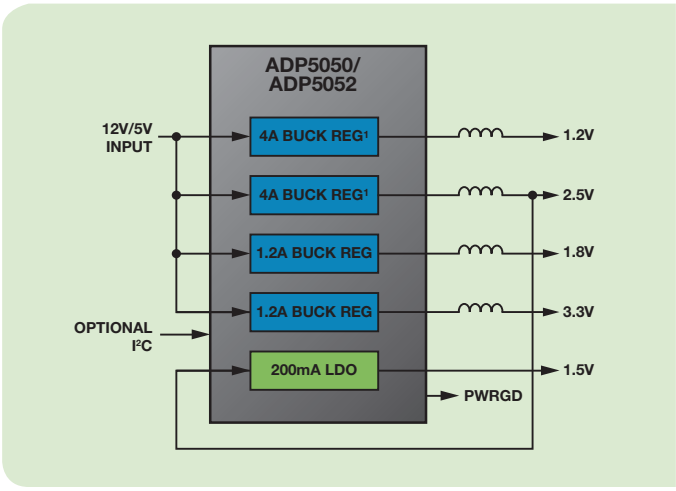
Integrated Power Management Solutions

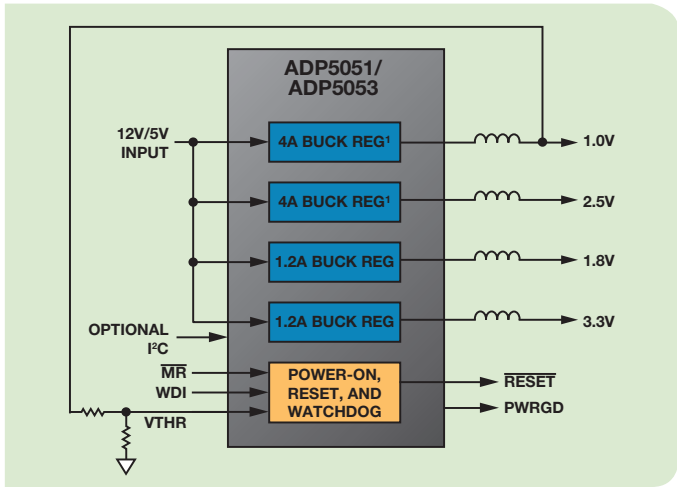
Analog Devices Announces a New Family of Multichannel Regulators



ANALOG DEVICES

Quad Buck Switching Regulator with LDO or POR/WDI in LFCSP



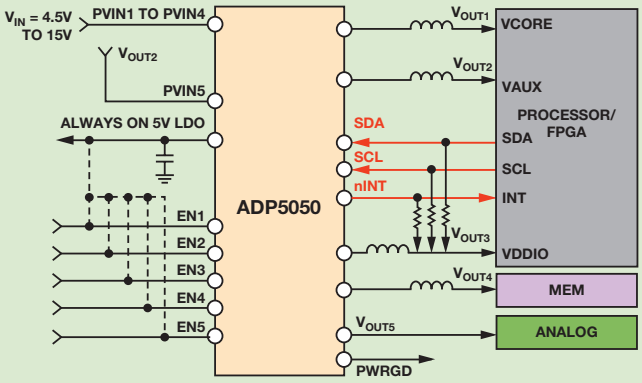


[1] Resistor programmable current limit (4 A, 2.5 A, or 1.2 A).

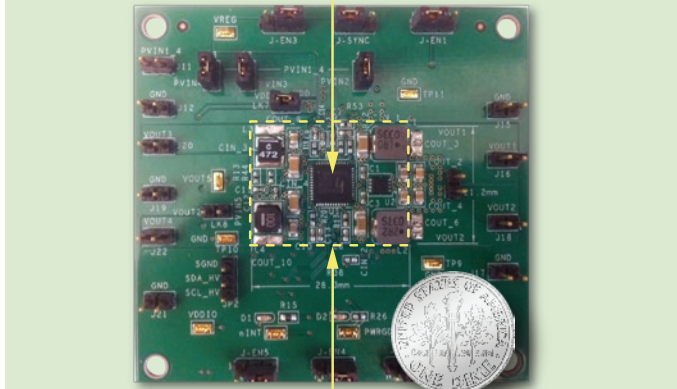
Key Features

- Wide input voltage range: 4.5 V to 15 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 1.4 MHz adjustable switching frequency
- Adjustable/fixed output options via factory
- Pseudo DVS (dynamic voltage scaling)
- I²C interface with interrupt supportive on fault condition
- CH1/CH2: programmable 1.2 A/2.5 A/4 A sync buck regulator with low-side FET driver
- CH3/CH4: 1.2 A sync buck regulator
- CH5: 200 mA low dropout LDO or watchdog timer and power-on reset
- Precision enable on 0.8 V accurate threshold
- Active output discharge switch
- FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag on selective channels
- Startup with the precharged output
- 7 mm × 7 mm, 48-lead LFCSP package
- −40°C to +125°C junction temperature
- I²C functionality

I²C Functionality



ADP5050 application diagram featuring the I²C interface.



ADP505x solution size only 28.3 mm × 21.2 mm.

Option 1: Resistor-programmable output voltage from 0.8 V to V_{IN} × 0.85

Option 2: Fixed output voltage with I²C programmability with these ranges for each channel

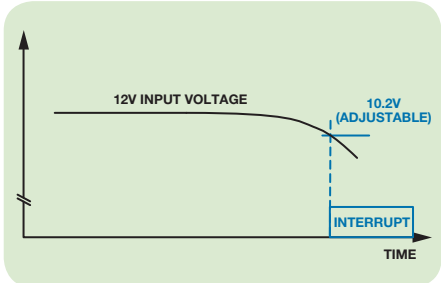
[CH1: 0.85 V TO 1.60 V, 25 mV STEP]

[CH2: 3.3 V TO 5.0 V, ~300 mV STEP]

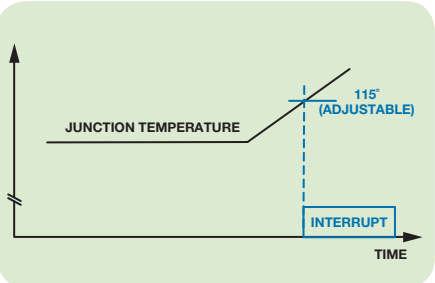
[CH3: 1.2 V TO 1.80 V, 100 mV STEP]

[CH4: 2.5 V TO 5.5 V, 100 mV STEP]

ADP505x output voltage options.



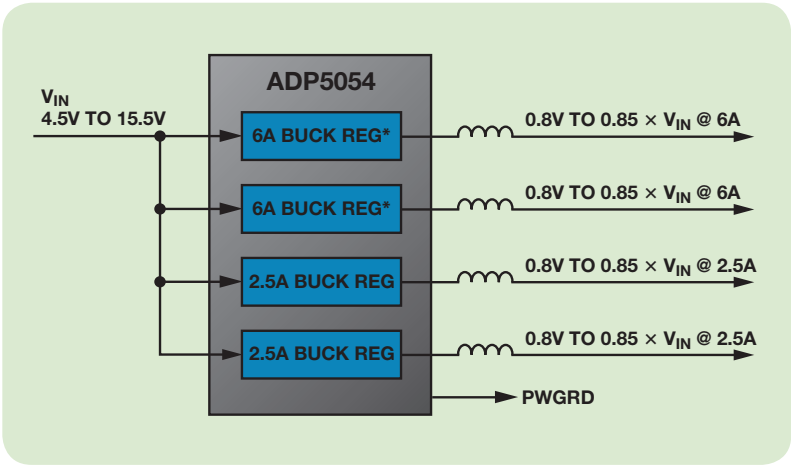
Low input voltage detection on PVIN1.



Overheat function on junction temperature.

ADP5054

Quad Buck Switching Regulator in LFCSP

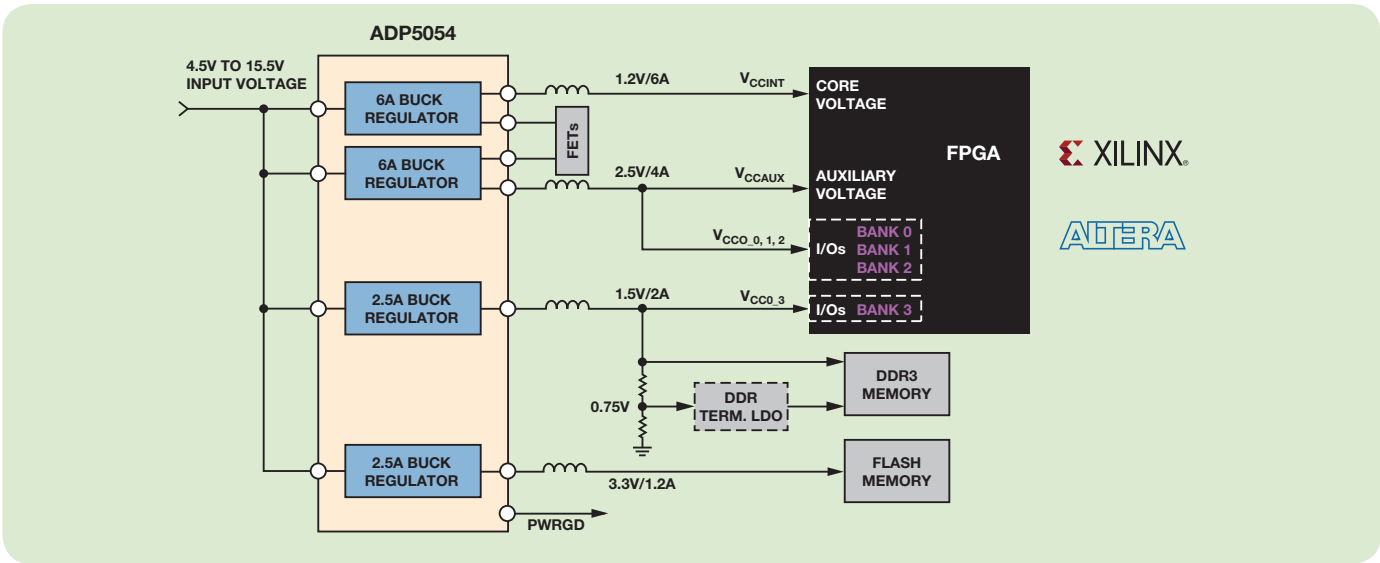


*Resistor-programmable current limit (6 A, 4 A, 2 A).

Key Features

- CH1/CH2: programmable 2 A/4 A/6 A sync buck regulator with low-side FET driver
  - Parallel CH1/CH2 to deliver up to 12 A output
- CH3/CH4: 2.5 A buck regulator
  - Parallel CH3/CH4 to deliver up to 5 A output
- Wide input range: 4.5 V to 15.5 V
- Resistor adjustable or fixed output voltage
- 250 kHz ~ 2 MHz adjustable switching frequency
- ½ × f_{SW} selective for each channel
- Precision enable on accurate 0.8 V threshold
- Programmable current limit in CH1/CH2
- Soft start timer programmable
- FPWM/PSM mode selection
- Active output discharge switch
- PWRGD flag on selective channels
- Frequency synchronization input or output
- Hiccup or latch-off for output short protection
- UVLO, OCP, TSD
- 7 mm × 7 mm, 48-lead LFCSP package

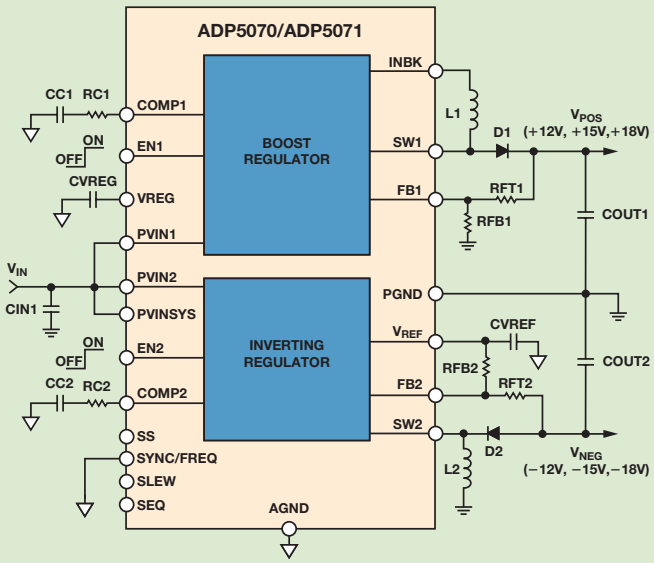
Power for FPGA Applications Example



Part Number	Number of Outputs	V_{IN} (V)	V_{OUT} (V)	Max Output Current (A)	Switching Frequency Range	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Package	Price 1k List ($U.S.)
ADP5050	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	—	—	—	48-lead LFCSP	4.39
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5051	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	4.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5052	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	—	—	—	48-lead LFCSP	3.59
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
	1 × 200 mA LDO	1.7 to 5.5	0.5 to 4.75	200 mA	—						
ADP5053	2 × 4 A[1] bucks	4.5 to 15	0.8 to 0.85 × V_{IN}	1.2/2.5/4[1]	250 kHz to 1.4 MHz	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	48-lead LFCSP	3.79
	2 × 1.2 A bucks		0.8 to 0.85 × V_{IN}	1.2							
ADP5054	2 × 6 A[2] bucks	4.5 to 15.5	0.8 to 0.85 × V_{IN}	6/4/2[2]	250 kHz to 2 MHz	—	—	—	—	48-lead LFCSP	4.29
	2 × 2.5 A bucks		0.8 to 0.85 × V_{IN}	2.5							

[1] Resistor-programmable current limit (4 A, 2.5 A, or 1.2 A).
[2] Resistor-programmable current limit (6 A, 4 A, or 2 A).

Dual Switching Regulator for Generating V_{POS} and V_{NEG} in LFCSP and TSSOP



- RESISTOR-PROGRAMMABLE (SYMMETRIC AND ASYMMETRIC)
- EXAMPLE OUTPUTS SUPPORTED: ±3V, ±5V, ±12V, ±10V, +15V, AND −10V
- APPLICATIONS: BIPOLAR AMPLIFIERS, ANALOG-TO-DIGITAL CONVERTERS AND DIGITAL-TO-ANALOG CONVERTERS, MULTIPLEXERS, AMPLIFIERS, CCDS AND OLEDS, RF PA BIAS SUPPLY, GaN FET BIAS, AND OPTICAL MODULES

Key Features:

- Wide input voltage range: 2.85 V to 15 V
- Generates well regulated, independently resistor-programmable V_{POS} and V_{NEG} outputs (for example, +15 V and −10 V)
- True shutdown for both positive and negative outputs
- 1.2 MHz/2.4 MHz switching frequency with optional external frequency synchronization from 1.0 MHz to 2.6 MHz
- Resistor-programmable soft start timer
- Individual precision enable and flexible start-up sequence control for symmetric start, V_{POS} first, or V_{NEG} first
- Boost and inverter, out of phase operation (180°)
- UVLO, OCP, OVP, and TSD protection
- Slew rate control for lower system noise
- 4 mm × 4 mm, 20-lead LFCSP or TSSOP-EP package
- −40°C to +125°C junction temperature
- Supported by ADIsimPower tool set

Boost Regulator—Positive Rail

- Adjustable positive output: up to +39 V
- Integrated 1.0 A/39 V main switch (ADP5070)
- Integrated 2.0 A/39 V main switch (ADP5071)
- Optional SEPIC configuration for automatic step-up/down

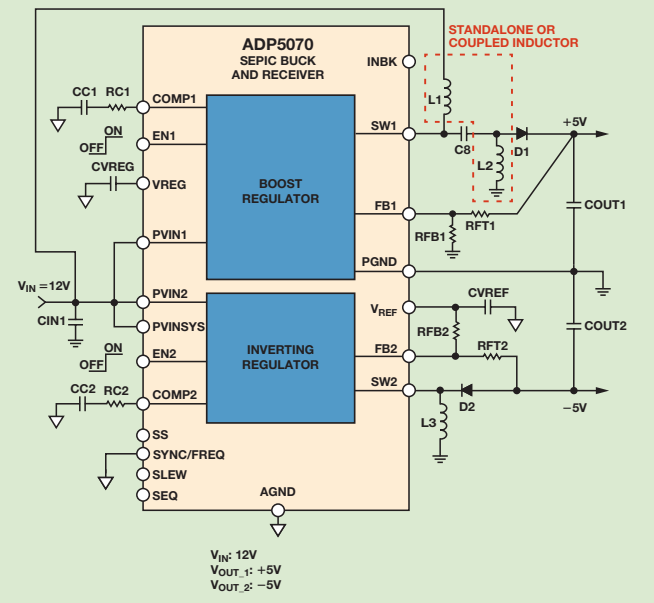
Inverter Regulator—Negative Rail

- Adjustable negative output: up to −39 V below V_{IN}
- Integrated 0.6 A/39 V main switch (ADP5070)
- Integrated 1.2 A/39 V main switch (ADP5071)

ADIsimPower

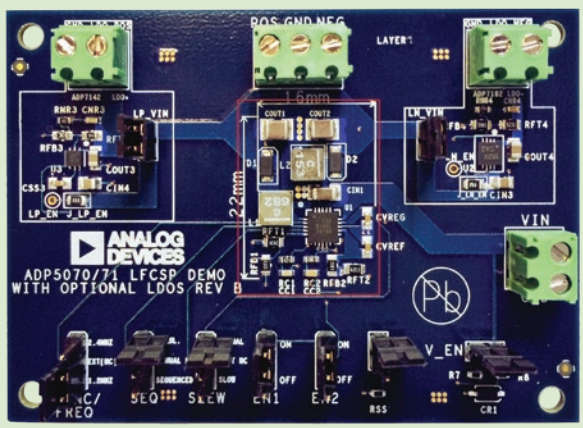
http://download.analog.com/PMP/ADP507x_designer.zip

SEPIC Configuration to Support Automatic Step-Up/Down Capability



- RESISTOR-PROGRAMMABLE (SYMMETRIC AND ASYMMETRIC)
- EXAMPLE OUTPUTS SUPPORTED: ±5V, ±3.5V, +3.3V, AND −2.5V

ADP5070/ADP5071 Demo Board



Part Number	V_{IN} (V)	V_{OUT} (V)	Number of Outputs	Output Current (mA)	Key Features	Package	Price ($U.S.)
ADP5070 *New*	Boost/inverter: 2.85 to 15	Boost: V_{IN} to 39 Inverter: –0.5 to –39 below V_{IN}	1 × boost 1 × inverter	Input current limit: boost: 1 A, inverter: 0.6 A	Individual enable pin, adjustable outputs, soft start, and slew rate	20-lead LFCSP, 20-lead TSSOP	2.19
ADP5071 *New*	Boost/inverter: 2.85 to 15	Boost: V_{IN} to 39 Inverter: –0.5 to –39 below V_{IN}	1 × boost 1 × inverter	Input current limit: boost: 2 A, inverter: 1.2 A	Individual enable pin, adjustable outputs, soft start, and slew rate	20-lead LFCSP, 20-lead TSSOP	2.39

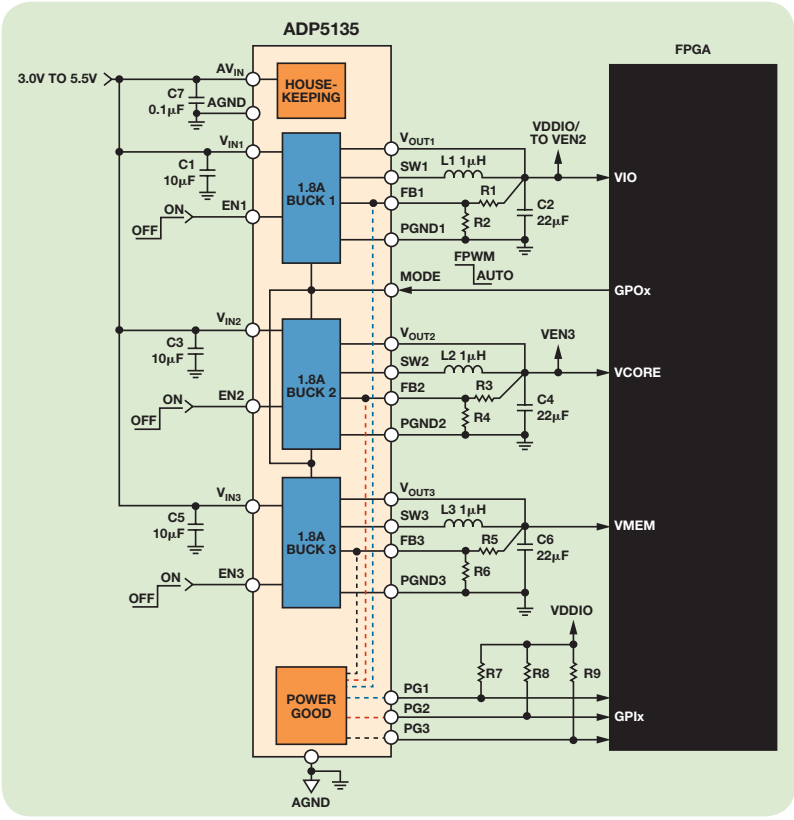
ADP5135: Triple, 1.8 A, 3 MHz Buck Regulator in LFCSP

Key Features

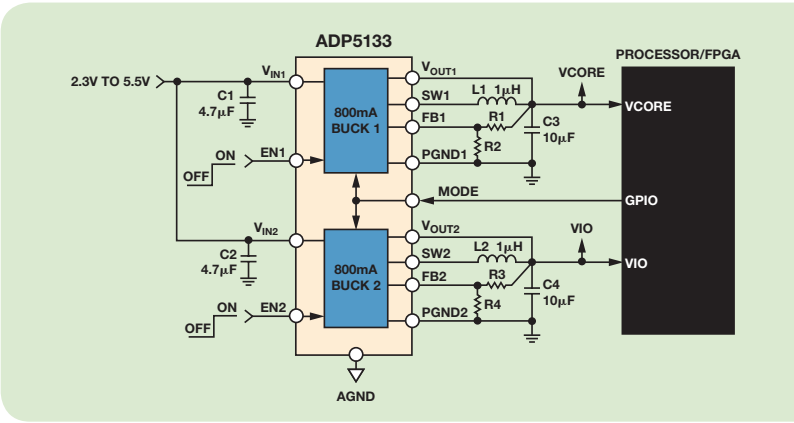
- Main input voltage range 3.0 V to 5.5 V
- Three 1800 mA buck regulators
- 4 mm × 4 mm, 24-lead LFCSP package
- Regulator accuracy of ±1.8%
- Individual, dedicated buck power good pins
- Precision enables pins for easier power sequencing
- 3 MHz buck operation with forced PWM and automatic PWM/PSM modes
- Buck output voltage range from 0.8 V to 3.8 V

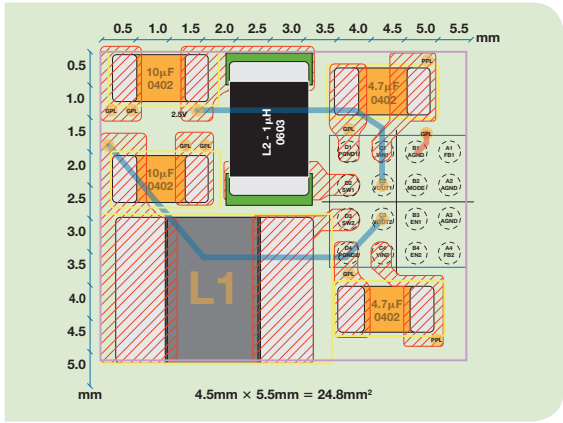
Applications

- Power for processors, application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and radio frequency (RF) chipsets



ADP5133: Dual 800 mA Buck Regulator in WLCSP





Key Features

- Input voltage range: 2.3 V to 5.5 V
- Two 800 mA buck regulators
- Adjustable and factory-programmable output voltages
  - Adjustable output voltage range: 0.8 V to 3.8 V
  - Fixed output voltage range: 0.9 V to 3.3 V
- Regulator accuracy: ±1.8%
- Overcurrent and thermal protection
- Soft start and undervoltage lockout
- Buck 1 and Buck 2 key specifications
  - Current mode architecture for excellent transient response and 100% duty operation
  - 3 MHz operating frequency
  - Forced PWM and auto PWM/PSM modes
  - Out of phase operation for reduced input filtering
- –40°C to +125°C junction temperature
- Tiny, 2 mm × 2 mm, 16-ball WLCSP package

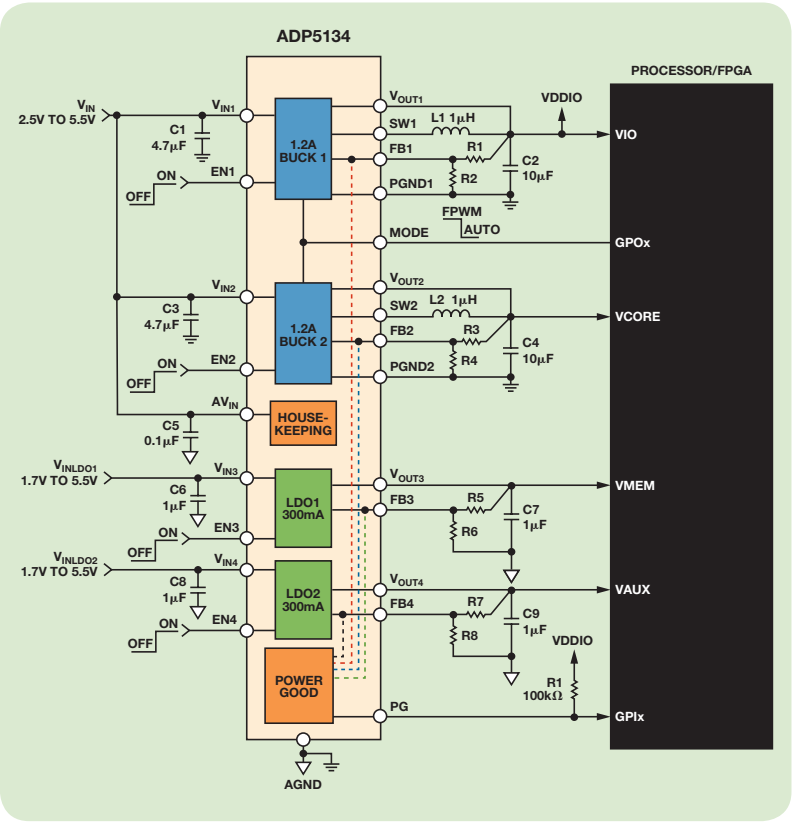
Dual, 3 MHz, 1.2 A Buck Regulator with Two 300 mA LDOs with Precision Enable and a Power Good in LFCSP

Key Features

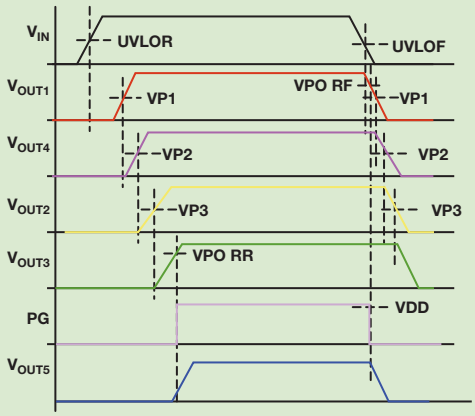
- Main input voltage range 2.5 V to 5.5 V
- Two 1200 mA buck regulators and two 300 mA LDO regulators
- 4 mm × 4 mm, 24-lead LFCSP package
- Regulator accuracy of ±1.8%
- Factory-programmable or external adjustable VOUTx
- Precision enables pins for easier power sequencing
- Factory selectable power-good pin
- 3 MHz buck operation with forced PWM and automatic PWM/PSM modes
- Buck 1/Buck 2: output voltage range from 0.8 V to 3.8 V
- LDO1/LDO2: output voltage range of 0.8 V to 5.2 V
- LDO1/LDO2: input voltage range from 1.7 V to 5.5 V
- LDO1/LDO2: high PSRR and low output noise

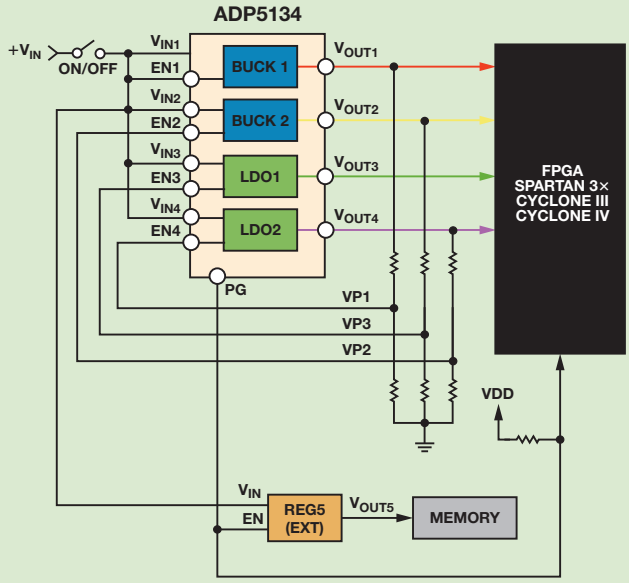
Applications

- Power for processors, application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and radio frequency (RF) chipsets



Sequencing and Power Good with ADP5134





Assumptions

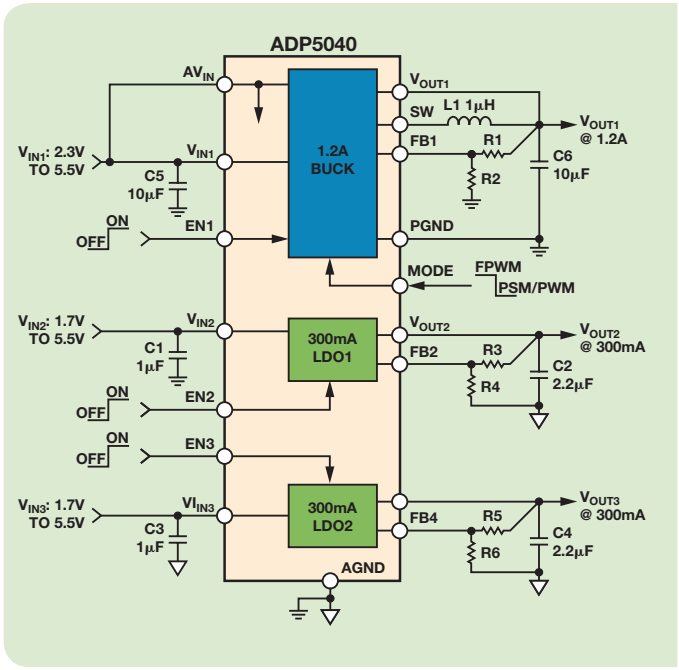
- Power good factory programmed to sense all regulators

Benefits

- Precise and reliable
- Few external components needed
- Minimal cost adder (resistors)
- Flexible sequencing

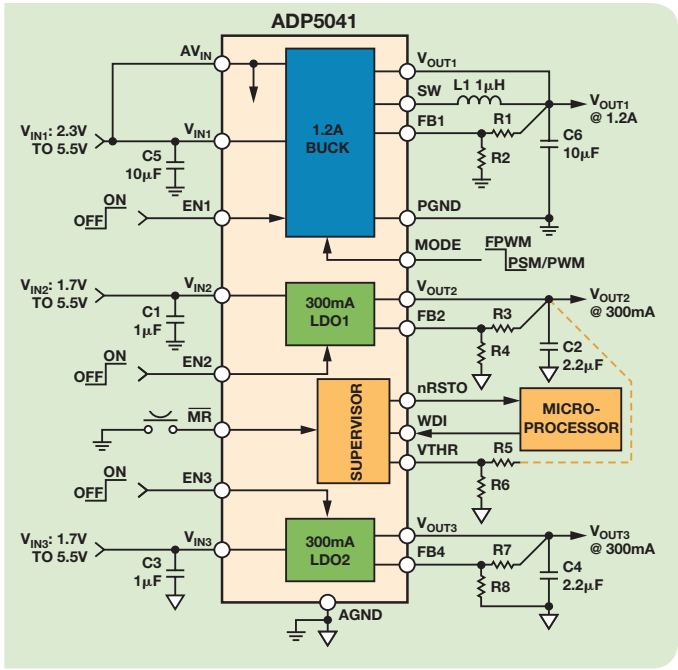
ADP5040 and ADP5041

ADP5040: 1.2 A Buck and Dual 300 mA LDO with Individual Enables in LFCSP



ADP5040 functional block diagram.

ADP5041: 1.2 A Buck and Dual 300 mA LDO, Supervisory, Watchdog, and Manual Reset in LFCSP



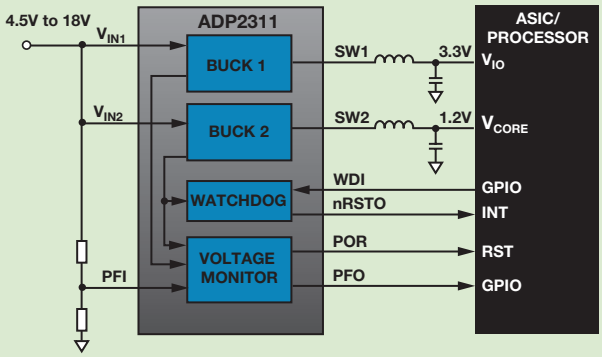
ADP5041 functional block diagram.

Key Features

- Input voltage range: 2.3 V to 5.5 V
- One 1.2 A buck regulator, fixed and adjustable output voltages, up to 96% efficiency
- Two 300 mA LDOs, fixed and adjustable outputs
- 4 mm × 4 mm, 20-lead LFCSP package
- Initial regulator accuracy: ±1%
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Open-drain processor reset with external adjustable threshold monitoring
- ±1.5% threshold accuracy over the full temperature range
- Guaranteed reset output valid to V_{CC} = 1 V
- Manual reset input
- Watchdog refresh input
- Two reset timeout options: 20 ms and 140 ms (minimum)
- Two watchdog timeout options: 102 ms and 1600 ms (typical)

ADP2311

Dual, 1 A Buck Regulators with Fail-Safe Monitoring



Key Features

- Input voltage: 4.5 V to 18 V
- Continuous output current: 1 A/1 A
- Output accuracy: ±1.0%
- Power fail comparator generates warning
- Power-on reset with programmable delay timer
- Adjustable voltage monitor for power-down (Channel 2)
- Watchdog refresh input
- Fixed switching frequency: 300 kHz
- Internal compensation and soft start
- Precision enable inputs
- Power feedback during power-off
- UVLO, OCP, OVP, and thermal shutdown protection
- 4 mm × 4 mm, 24-lead LFCSP package

Applications

- Industrial and instrumentation
- Healthcare and medical
- DC-to-DC point of load applications

Integrated Power Management Solutions (Micro-PMUs)

Part Number	Product Description	V_{IN} (V)	V_{OUT} (V)	Number of Outputs	Output Current (mA)	I²C	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Key Features	Package	Price ($U.S.)
ADP5022	Dual, 3 MHz buck with 150 mA LDO	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8	2 × buck	600	—	—	—	—	Mode pin, individual enable pins	16-ball WLCSP	1.80
		LDO: 1.7 to 5.5	LDO: 3.3, 3.0, 2.9, 2.8, 2.775, 2.5, 2.0, 1.875, 1.8, 1.75, 1.7, 1.65, 1.6, 1.55, 1.5, 1.2	1 × LDO	150							
ADP5023	Dual, 800 mA buck with 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.59
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	1 × LDO	300							
ADP5024	Dual, 1.2 A buck with 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.79
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	1 × LDO	300							
ADP5033	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	2 × buck	800	—	—	—	—	Mode pin, two enable pins	16-ball WLCSP	1.90
		LDO: 1.7 to 5.5	LDO: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1.0, 0.9, 0.8	2 × LDO	300							
ADP5034	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP, 28-lead TSSOP	1.99
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5133 ***New***	Dual, 3 MHz buck regulator	Buck: 2.3 to 5.5	Adj (0.8 to 3.8) or 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9	2 × buck	800	—	—	—	—	Adjustable and fixed outputs	16-ball WLCSP	1.29
ADP5134 ***New***	Dual, 3 MHz buck regulator with dual LDO	Buck: 2.5 to 5.5	Adj (0.8 to 3.8)	2 × buck	1200	—	—	—	—	Precision enable pins and power-good pin	24-lead LFCSP	2.09
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5135 ***New***	Triple, 3 MHz buck regulator	Buck: 3.0 to 5.5	Adj (0.8 to 3.8)	3 × buck	1800	—	—	—	—	Precision enable pins and power-good pins	24-lead LFCSP	1.69
ADP5037	Dual, 3 MHz, 800 mA buck regulator with dual 300 mA LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	2 × buck	800	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.69
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5040	3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	—	—	—	Individual enable pins, mode pin	20-lead LFCSP	1.39
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5041	3 MHz buck regulator with dual LDO, supervisor, and watchdog timer	Buck: 2.3 to 5.5	Adj (0.8 to 3.8)	1 × buck	1200	—	0.5 (adj)	20, 140	102, 1600	Individual enable pins and supervisor, WDI, mode pin, and MR pin	20-lead LFCSP	1.79
		LDO: 1.7 to 5.5	Adj (0.8 to 5.2)	2 × LDO	300							
ADP5070 ***New***	Dual dc-to-dc with boost and inverter outputs for generating V_{POS} and V_{NEG}	Boost/inverter: 2.85 to 15	Boost: V_{IN} to 39	1 × boost	Input current limit: boost: 1 A inverter: 0.6 A	—	—	—	—	Individual enable pin, adjustable outputs, soft start, and slew rate	20-lead LFCSP, 20-lead TSSOP	2.19
			Inverter: –0.5 to –39 below V_{IN}	1 × inverter								
ADP5071 ***New***	Dual dc-to-dc with boost and inverter outputs for generating V_{POS} and V_{NEG}	Boost/inverter: 2.85 to 15	Boost: V_{IN} to 39	1 × boost	Input current limit: boost: 2 A inverter: 1.2 A	—	—	—	—	Individual enable pin, adjustable outputs, soft start, and slew rate	20-lead LFCSP, 20-lead TSSOP	2.39
			Inverter: –0.5 to –39 below V_{IN}	1 × inverter								
ADP5073 ***New***	Inverting switching regulator for generating V_{NEG}	Inverter: 2.85 to 15	Inverter: –0.5 to –39 below V_{IN}	1 × inverter	Inverter: 1.2 A	—	—	—	—	Enable pin, adjustable output, soft start, and slew rate	16-lead LFCSP	1.49
ADP5074 ***New***	Inverting switching regulator for generating V_{NEG}	Inverter: 2.85 to 15	Inverter: –0.5 to –39 below V_{IN}	1 × inverter	Inverter: 2.4 A	—	—	—	—	Enable pin, adjustable output, soft start, and slew rate	16-lead LFCSP	1.75
ADP5075 ***New***	Inverting switching regulator for generating V_{NEG}	Inverter: 2.85 to 15	Inverter: –0.5 to –39 below V_{IN}	1 × inverter	Inverter: 0.6 A	—	—	—	—	Enable pin, adjustable output, soft start, and slew rate	12-ball WLCSP	0.99
ADP5050 ***New***	Quad buck regulator with LDO with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	—	—	—	I²C interface with individual enable pins and power good	48-lead LFCSP	4.39
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5051 ***New***	Quad buck regulator, POR, and WDI with I²C	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	Yes	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	I²C interface with individual enable pins and power good	48-lead LFCSP	4.59
				2 × buck	1200							
ADP5052 ***New***	Quad buck regulator with LDO	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	—	—	—	Individual enable pins with power good	48-lead LFCSP	3.59
				2 × buck	1200							
		LDO: 1.7 to 5.5	0.5 to 4.75	1 × LDO	200							
ADP5053 ***New***	Quad buck regulator with POR and WDI	Buck: 4.5 to 15	0.8 to 0.85 × V_{IN}	2 × buck	4000[1]	—	0.5 (adj)	1, 20, 140, 1120	6.3, 102, 1600, 25,600	Individual enable pins with power good	48-lead LFCSP	3.79
				2 × buck	1200							
ADP5054 ***New***	Quad buck regulator	Buck: 4.5 to 15.5	0.8 to 0.85 × V_{IN}	2 × buck	6000[2]	—	—	—	—	Individual enable pins with power good	48-lead LFCSP	4.29
				2 × buck	2500							
ADP2311 ***New***	Dual 1 A buck	4.5 to 18	Adj, (0.6 to 0.85 × V_{IN})	2 × buck	1000	—	0.95 × V_{FB}	Adj	50, 100,150, 200	PFO, PFI, WDI	24-lead LFCSP	2.38

[1] Resistor-programmable current limit (4 A, 2.5 A, or 1.2 A).
[2] Resistor-programmable current limit (6 A, 4 A, or 2 A).

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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