Embedded Processors and DSP Selection Guide 2012

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Embedded Processors and DSP
Selection Guide 2012

BlackFin®

SHARC®

DSP PERFORMANCE AUDIO

TigerSHARC®

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ADI Embedded Processors Portfolio

Analog Devices embedded architectures feature simple yet powerful programming models and are supported by high quality development tools.

Blackfin Processors

High Performance, Low Power Processing

Blackfin® processors embody a new breed of embedded processors designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. Blackfin processors deliver breakthrough signal processing performance and power efficiency with a RISC programming model. Blackfin processors present high performance, homogeneous software targets that allow flexible resource allocation between hard real-time DSP tasks and nonreal-time control tasks. System control tasks can often run in the shadow of DSP and video tasks.

Blackfin Processors Are Ideal For:

- Portable and networked digital media appliances
- Consumer communications and networks
- Automotive telematics, safety driver assistant, and infotainment
- Industrial instrumentation and medical equipment

SHARC Processors

Leadership in Floating-Point Applications

SHARC® processors offer exceptionally high floating-point DSP performance while integrating application-specific peripherals and interfaces designed to minimize overall system costs. The completely code-compatible family portfolio extends from entry-level products that are priced under $10 to high-end products providing 450 MHz/2.7 GFLOPS of signal processing performance. The broad range of price and performance points available in the SHARC processor family makes its members particularly well-suited to applications ranging from consumer, automotive, and professional audio to industrial and medical applications.

All SHARC processors are based on a 32-bit Super Harvard Architecture that combines a high performance signal processing core with sophisticated memory and I/O processing subsystems. This balanced architecture enables unparalleled performance while ensuring that sufficient memory and I/O bandwidth are available for the most algorithmically challenging applications. In addition to these hardware-centric efficiencies, all SHARC processors offer a very flexible algorithm development environment by supporting a variety of fixed- and floating-point data types.

The latest members of the SHARC family off load some of the most frequently used and intensive processing into hardware accelerators. An accelerator dedicated for filter processing can reduce the MIPS load on the core, freeing it up for other tasks. The FIR/IIR/FFT accelerator units are capable of performing the filters and FFT without core intervention. This gives software developers enormous freedom to use the core MIPS to implement complex algorithms, effectively adding more MIPS to the processor.

SHARC Processors Are Ideal For:

- Home theater audio systems
- Professional audio systems
- Automotive audio systems
- Industrial and instrumentation equipment
- Medical imaging
- Telephony

SigmaDSP Audio Processors

SigmaDSP® processors are fully programmable, single-chip audio DSPs that are easily configurable through the SigmaStudio™ graphical development tool, and are ideal for automotive and portable audio products. SigmaDSP chips are available with integrated sample rate converters, ADCs, DACs and output amplifiers.

SigmaDSP Processors Are Ideal For:

- Portable audio applications
- Automotive audio systems
- Consumer audio applications

TigerSHARC Processors

Highest Performance Multiprocessor Systems

The TigerSHARC® processor family offers the industry's highest performance per watt and per square inch of board space for the most demanding signal and image processing applications. Its patented link port technology allows glueless interprocessor communication within arrays of two or more TigerSHARC processors, delivering unbounded performance in terms of MMACS and MFLOPS.

Based on a 128-bit static superscalar architecture, TigerSHARC processors offer native support of fixed- and floating-point data types and a balanced combination of computational performance, I/O bandwidth, and memory integration. Together, this yields sustained DSP system-level performance that is two to four times greater than conventional DSPs or microprocessors with vector processing units.

By providing native support for 1-bit data formats used for chip-rate processing, TigerSHARC processors pioneer a new class of software-defined radios and serve applications that were previously the exclusive domain of expensive ASICs (application-specific integrated circuits) and FPGAs (field-programmable gate arrays). In addition, by moving to a software-centric design model, TigerSHARC processors allow IP reuse, which greatly enhances R&D productivity throughout each successive product generation.

TigerSHARC Processors Are Ideal For:

- Wireless infrastructure WiMAX applications such as 802.16 and other advanced standards (e.g., OFDM), base stations, and software-defined radios
- Floating point, performance density related systems in both the single and multiprocessor environments
- Medical imaging equipment (e.g., CAT scan, ultrasound, and MRI)
- Military equipment (e.g., radar/sonar, munitions targeting, and optoelectronics)
- Industrial and instrumentation equipment
- Automated test equipment

Markets and Applications

Market	Applications	Architecture/Platform
Communications		
Broadband	Broadband Over Power Lines	Blackfin
	Digital Media Gateways (VOD)	Blackfin
	Home Networking	Blackfin
	IP PBX	Blackfin
	IP Set-Top Box	Blackfin
	Media Node	Blackfin
	Multimedia Over IP	Blackfin
	Video Conferencing/Phone	Blackfin
	Video Surveillance/Security	Blackfin
	Voice Over IP	Blackfin
Wireless	Access (Broadband) (i.e., 802.16 ...)	Blackfin, TigerSHARC
	Base Station	TigerSHARC
	Cellular Location	Blackfin
	Satellite Phone	Blackfin
	Handset Audio/Accessories	SigmaDSP
Automotive		
In Cabin	Audio Amplifier	SHARC, SigmaDSP
	Audio Jukebox	Blackfin
	Digital Radio	Blackfin
	Driver Assistance	Blackfin
	Handsfree	Blackfin
	Head Unit	Blackfin, SHARC, SigmaDSP
	Multimedia Device Interface	Blackfin
	Navigation	Blackfin, SigmaDSP
	Occupancy/Classifications	Blackfin
	Premium Audio System	SHARC
	Rear Seat Audio/Video	Blackfin, SigmaDSP
Consumer		
Security	Biometrics	Blackfin, SHARC
	Video Surveillance	Blackfin
Entertainment	Digital Home Video Appliance	Blackfin
	Digital Network Media Devices	Blackfin
	Digital Radio	Blackfin
	Digital Still Camera	Blackfin, SigmaDSP
	Digital TV (Audio)	Blackfin, SHARC, SigmaDSP
	Digital Video Camera	Blackfin
	Digital Video Recorder	Blackfin
	DVD/HD DVD/Blu-ray	SHARC
	Home Server	Blackfin, SHARC
	Home Theater A/V Receiver	SHARC
	Wireless Headphones/Headsets	Blackfin
	IP Set-Top Box	Blackfin
	Networked A/V Receiver	Blackfin
	Portable Media Player/ Portable Entertainment Console	Blackfin, SigmaDSP
	Portable Navigation	SigmaDSP
	Multimedia Accessories	Blackfin, SigmaDSP
	Professional Audio/Broadcast	SHARC
	Professional Audio/Music Products	Blackfin, SHARC, SigmaDSP
	Prosumer Audio	SHARC
	Satellite Radio	Blackfin
Toys	Interactive Toys	Blackfin
	Video Game Console	Blackfin

Market	Applications	Architecture/Platform
Industrial and Instrumentation		
Medical	CT	Blackfin, SHARC, TigerSHARC
	Diagnostic	Blackfin, SHARC, TigerSHARC
	MRI	SHARC, TigerSHARC
	Patient Monitoring	Blackfin, SHARC, TigerSHARC
	Portable Medical	Blackfin, SHARC
	Ultrasound	Blackfin, SHARC, TigerSHARC
	X-Ray	SHARC, TigerSHARC
Point of Sale	Scanner	Blackfin
	Vending Machine	Blackfin
Test/ Measurement Equipment	ATE	Blackfin, SHARC, TigerSHARC
	Communications	Blackfin, SHARC, TigerSHARC
	Measurement	Blackfin, SHARC, TigerSHARC
Industrial	Data Acquisition	Blackfin, SHARC
	Factory Automation	Blackfin
	Industrial Control	Blackfin, SHARC, TigerSHARC
	Machine Control	Blackfin
	Metering	Blackfin
	Motor Control	Blackfin
	Network Management	Blackfin
	Power Control	Blackfin
	Power Inverters	Blackfin
	Robotics	Blackfin, SHARC, TigerSHARC
	Verification and Biometrics	Blackfin
	Video Surveillance Systems	Blackfin
	Vision Systems	Blackfin
Military/Aerospace		
Guidance	Radar	SHARC, TigerSHARC
	Sonar	SHARC, TigerSHARC
Aerospace	Control	Blackfin
	Entertainment	Blackfin
Military	Avionics	Blackfin, SHARC, TigerSHARC
	Communications	Blackfin, TigerSHARC
	Digital Radio	Blackfin, SHARC, TigerSHARC
	Location	Blackfin, TigerSHARC
	Military Imaging	TigerSHARC
	Radar/Sonar	SHARC, TigerSHARC
	Smart Munitions	TigerSHARC
	Target Detection	TigerSHARC

Technical Workshops and University Program

Technical Workshops

Cut your time to market by getting up to speed fast. The embedded processing and DSP system development and programming workshops provide comprehensive hands-on training on Analog Devices embedded processors and DSPs. The workshops are geared toward people who have a working knowledge of microprocessors and want to learn how to use Analog Devices embedded processors and DSPs. These courses cover the DSP architecture, assembly language syntax, I/O interface, hardware, and software development tools. Throughout the workshop, attendees learn how easy it is to use Analog Devices embedded processors and DSPs from lecture sessions and hands-on exercises.

1-Day Workshops and Seminars

Workshops and seminars for those who want to evaluate the capabilities of ADI high performance embedded processors and development tools. Practical issues and concerns will be addressed in addition to the strengths and power of these devices.

Multiday Workshops

In-depth technical training designed to develop a strong working knowledge of embedded processors and development tools through lecture and hands-on exercises. Workshops are typically 3.5 days and presented by Kaztek Engineering's ADI-trained instructors.

University Workshops

These workshops are presented by ADI's worldwide university network and are taught by local university professors who are supported by Analog Devices embedded processor and DSP application teams.

For more information and schedules, visit
www.analog.com/processors/workshops.

ADI Embedded Processing and DSP University Program

The Analog Devices DSP University Program promotes embedded and digital signal processing education and research at engineering institutions worldwide. It provides the next generation of engineers with embedded processing and DSP knowledge to help them compete in the industry of tomorrow.

Benefits of the ADI DSP University Program

- Lab recommendations
- Complete software and hardware tools to set up an embedded processor or DSP lab
- Discounts on development tools
- Discounts of up to 90% on hardware and software development tools
- Teaching resources
  - Sample lectures and labs
- Discounts on ADI embedded processor and DSP workshops
  - In-depth, hands-on, 3.5-day training sessions

Analog Devices Technologies Are Ideally Suited for Teaching

- Embedded processor and DSP architectures that are the simplest in the industry to program
- Simple instruction sets
- High level of SRAM integration

To learn more about the program and available discounts, visit
www.analog.com/processors/university.

Online Training

Visual Learning and Development

Master the incredible potential of the Blackfin, SHARC, and SigmaDSP processors and build better applications. Discover how—without ever leaving your desk—by taking one of the new Blackfin, SHARC, or SigmaDSP online training modules.

The modules cover a wide range of topics that address different stages of your development cycle—from the fundamentals of Analog Devices' development tools to tips on how developers can optimize their system performance. These modules are designed to be used independently or in combination, depending on the experience and interest of the viewer.

Video Training Modules

ADI in Applications

New SHARC Processors for HD Audio Applications

Overview of ADI's new 400 MHz SHARC ADSP-2148x series processors for HD audio and home theater applications. Renowned in the pro audio market for enabling exquisite sound quality and advanced digital effects, this video highlights how SHARC-caliber processing can now be applied to consumer AVR systems requiring low cost, single-chip implementations.

New SHARC Processors for Healthcare Applications

ADI's new low power SHARC ADSP-2147x floating-point processor brings portability to sophisticated medical instrumentation. This overview highlights how the SHARC ADSP-2147x series optimizes power budget-sensitive portable medical system design ranging from medical imaging equipment to patient monitoring devices.

New SHARC Processors for Industrial Applications

ADI's new 400 MHz SHARC ADSP-2148x processor series brings high performance native floating-point processing to a new cost point for products in test and measurement, renewable energy, motor control, and smart grid applications.

Processors in Test, Measurement, and Control

This 43-minute engineer-to-engineer session provides an overview of the test measurement and control (TM&C) market, specifically geared towards the value of programmable processors. During this module, you will find information on Analog Devices processor families and the value each of the architectures brings into the four categorized markets. Besides processor value, this training module contains highlights of different applications where these processors have been and continue to be used. Finally, a highlight on some partners and the value they bring into the market and how these are helpful when deploying a solution on TM&C.

ADI Solutions for Video Surveillance Equipment

This 50-minute module provides an overview of Analog Devices products and solutions, including the Blackfin processor, for various video surveillance applications in the security market. Signal chain overviews of the broad ADI portfolio, as well as key partners, are included.

Processors in Portable Healthcare

This 15-minute module provides an overview of the evolving trends and requirements within select portable healthcare applications, mainly EKG, ECG, and AEG. It features the Blackfin processor portfolio and highlights the solutions it helps customers achieve when designing solutions for these applications. A key development partner is also featured.

Getting Started

Highlights of New SHARC Processor Families

This module highlights the industry-leading features of the new SHARC floating-point processor families, including fastest industry performance, lower price point, 5 Mb on-chip memory, and low power consumption.

Introduction to the SHARC EZ-KIT Lite Products (ADSP-2147x and ADSP-2148x)

Get your new SHARC processor design started quickly by familiarizing yourself with the capabilities of the EZ-Kit Lite® evaluation/development platform. Three example applications are demonstrated that leverage ADIs broad library of downloadable algorithms and software code modules.

SHARC ADSP-21469 EZ-KIT Lite Overview

This 3-minute video features an overview of the new SHARC ADSP-21469 EZ-KIT Lite evaluation platform. It provides an in-depth review of the EZ-KIT contents, including cables and development tools, and it also provides a detailed overview of the development board layout and functionality.

SHARC Processor Overview

This 46-minute engineer-to-engineer session provides an overview of the SHARC processor family. During this module, you will find information on the value the SHARC architecture brings to a variety of applications. This presentation will not go into deep technical details but will cover the architecture of the SHARC at a fairly high level. You will also be provided with information about available hardware and software development tools from Analog Devices to assist with product development.

SHARC ADSP-2146x Overview

This 60-minute module provides an overview of the SHARC ADSP-2146x processors, the newest members of the SHARC processor family. It provides an in-depth look at the key features of the ADSP-2146x family, such as variable instruction size execution, DDR2 DRAM controller, thermal diode, and media local bus interface. Recommended viewing if this is the user's first look at the SHARC processor family.

ADZS-ICE-100B Blackfin JTAG Emulator Overview

This 2-minute video provides an overview of the new ADZS-ICE-100B JTAG emulator for the Blackfin processor family, including a review of key features and functionality as well as ordering information.

Blackfin ADSP-BF506F EZ-KIT Lite Overview

This 3.5-minute video features an overview of the new Blackfin ADSP-BF506F EZ-KIT Lite evaluation platform. It provides an in-depth review of the EZ-KIT contents, including cables and development tools. It also provides a detailed overview of the development board layout and functionality.

Online Training

Blackfin Core Architecture

This module introduces the Blackfin family, which includes the Blackfin processors, tools, and other development support that is available.

Introduction to VisualDSP++ Tools

This module will give the user an overview of the VisualDSP++ Tools. For demonstration purposes, the ADSP-BF537 EZ-KIT Lite will be used as the target. Users will learn some quick tips on how to analyze and fine tune their applications.

Basics of Building a Blackfin Application

This module describes the basic software build process of VisualDSP++, specific Blackfin programming "gotchas," and basic code optimization strategies. Users will see an example demonstrating "zero effort" optimization by using built-in optimizer and cache.

Interfacing Blackfin with Audio and Video Peripherals

This module will familiarize the user with the principles behind connecting Blackfin processors to audio and video devices. It is recommended that users have some basic working knowledge of audio and video fundamentals.

Introduction to VDK

This 27-minute module provides an overview of the VisualDSP++ kernel. A demonstration shows the basics of building and debugging VDK projects. Users should have previous experience with operating systems, as well as a basic knowledge of software terminology.

Multimedia Starter Kit

This 52-minute module introduces the Multimedia Starter Kit. A demonstration covers JPEG and MJPEG. Users should have previous experience with embedded systems, basic knowledge of software terminology, and familiarity with VisualDSP++, Blackfin processors, and ADI evaluation boards.

Developing on ADI Processors

Lockbox Secure Technology on Blackfin Processors

This module focuses on the highlights of Lockbox® technology on Blackfin processors.

Blackfin Optimizations for Performance and Power Consumption

This module is about optimizing your software design for the Blackfin processor for better performance and lower power consumption.

Blackfin System Services

This module discusses the system services software available for Blackfin processors. It is recommended that users have some understanding of the Blackfin architecture, basic knowledge of software terminology, and experience in embedded systems.

Blackfin Device Drivers

This module discusses the device driver model for the Blackfin family of processors. It is recommended that users have an understanding of the Blackfin architecture and are familiar with the Blackfin system services software.

Rapid Development of a Blackfin-Based Video Application

This module discusses the rapid development process of a Blackfin video application using readily available and fully supported software and hardware modules. It is recommended that users understand the basic knowledge of software terminology, have experience in embedded systems, and understand Blackfin systems services and device drivers.

Using System Services Library and Device Drivers with VisualDSP++ Kernel in Blackfin Applications

This 50-minute module walks through the development of a Blackfin project that uses the system services library and device drivers (SSL/DD) in conjunction with the VisualDSP++ Kernel (VDK).

Advanced Topics

Programming and Optimizing C Code on Blackfin Processors

This module introduces concepts, tools, and approaches to optimizing Blackfin C applications. It highlights the problems and opportunities that can lead to potential performance improvements and reviews the available tools/techniques. The module covers a wide range from automatic optimization to detailed rewriting of C expressions.

Performance Tuning on the Blackfin Processor

This module discusses the techniques users can use to tune system performance for Blackfin processors. Users should have some understanding of the Blackfin architecture, a basic knowledge of software terminology, and experience in embedded systems.

New modules are in development. To view the latest modules available or take a training module, visit www.analog.com/VLD.

SigmaStudio Training

SigmaStudio™ training videos are available on ADI's video channel. These include many short courses on specific features, as well as tips for getting the most out of the tool and quickly developing a signal flow for your application.

Development Tools: CROSSCORE

Analog Devices CROSSCORE® development tools are focused on providing easier and more robust methods for engineers to develop and optimize systems by shortening product development cycles to reduce time to market.

- VisualDSP++ development environment
- EZ-KIT Lite evaluation kits
- EZ-Extender® daughter boards
- Emulators
- EZ-Board™ evaluation board
- Debug agent board

VisualDSP++ Integrated Development Environment

VisualDSP++ is an easy-to-install, easy to use, integrated software development and debugging environment (IDDE). More in-depth information is available on Page 10.

EZ-KIT Lite Evaluation Kit

These systems consist of a standalone evaluation board and an evaluation suite of VisualDSP++ to facilitate architecture evaluations via a PC-hosted tool set. Users can evaluate ADI's processors, learn about digital signal processing applications, as well as simulate, debug, and prototype applications.

EZ-Extender Daughter Boards

EZ-Extender daughter boards give developers access to and the ability to connect to various peripherals from Analog Devices and third parties via the expansion interface of the EZ-KIT Lite evaluation kits.

Emulators

Analog Devices cost-effective and high performance emulators provide an easy, portable, nonintrusive, target-based debugging solution for Analog Devices JTAG processors and DSPs. These powerful emulators perform a wide range of emulation functions, including single-step and full speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents.

See the Development Tools Table on Page 13 for available tools for Blackfin and SHARC processors.

EZ-Board Evaluation Boards

The EZ-Board evaluation board provides developers with a low cost platform for initial evaluation of the processors via an external emulator or μClinux.® The EZ-Board has an expansion interface that allows for modularity with different expansion board types with and without debug agents. The interface also provides a solution to user defined pins reserved for specific processor types and EZ-KIT Lite evaluation kits, multifunction pins, signal terminations, buffering, timing, and interface guidelines.

Debug Agent Board

The standalone debug agent is intended to provide a modular low cost emulation solution for EZ-Board evaluation boards as well as evaluation boards designed by third parties. The standalone debug agent is very similar to the debug agent that is on existing EZ-KIT Lite evaluation kits but has the flexibility to move from one board to another board.

VisualDSP++
Integrated Development Environment

Features

Integrated Development and Debugging Environment

- Supports all Analog Devices processors and DSPs
- Multiple project management
- Profiling and tracing of instruction execution
- Automation API and automation aware scripting engine
- Multiple processor support
- Background telemetry channel (BTC) support with data streaming capability
- Statistical profiling
- Graphical plotting capabilities
- Cache visualization
- Execution pipeline viewer
- Compiled simulation

Efficient Application Code Generation

- Native C/C++ compiler and enhanced assembler
- Profile guided optimization (PGO)
- Expert linker with profiling capability
- Integrated source code control
- TCP/IP and USP support for Blackfin processors
- Processor configuration/start-up code wizard for Blackfin processors
- VisualDSP++ Kernel (VDK) with multiprocessor messaging capability
- System services and device driver support for Blackfin processors
- File system support for Blackfin processors

Platform and Processor Support

VisualDSP++ Release 5.0 supports Analog Devices Blackfin processor, TigerSHARC processor, and SHARC processor families. Windows® XP, Windows 2000, and Windows Vista® hosts are supported.

Description	Part Number
VisualDSP++ Test Drive 90-day free trial	VDSP-BLKFN-PC-TEST
	VDSP-TS-PC-TEST
	VDSP-SHARC-PC-TEST

VisualDSP++ Development and Debugging Environment

VisualDSP++ is a state-of-the-art software development environment targeting the Analog Devices embedded processor portfolio. With the embedded software engineer and signal-processing-intensive applications specifically in mind, VisualDSP++, coupled with Analog Devices in-circuit emulator (ICE) and EZ-KIT Lite evaluation products, provides best-in-class capabilities for developing demanding real-time applications.
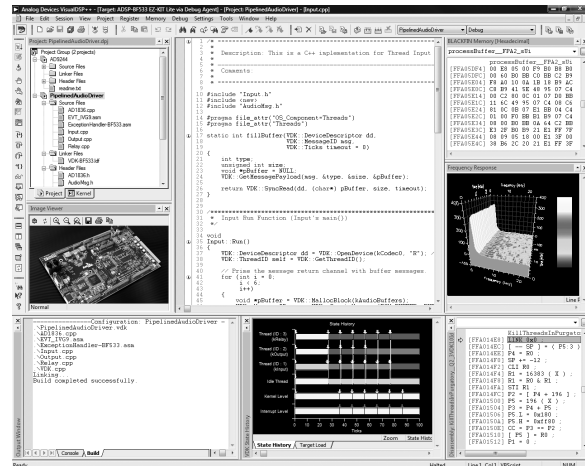
VisualDSP++ interface.

Develop High Performance Applications Quickly

At the heart of VisualDSP++ is a robust and powerful C/C++ compiler. The compiler consistently delivers industry-leading performance on standard benchmarks, ensuring that all but the most performance-demanding applications can be written entirely in the C language, accelerating development time while maintaining a portable code base. The compiler is backed by a rich library of signal-processing routines, allowing easy access to hand-coded, optimized implementations of FFTs, FIRs, etc. The Blackfin and SHARC compilers support MISRA-C:2004 for safety-critical embedded systems (*www.misra-c.com*).

The ANSI-C compiler is also augmented with popular language extensions and enhancements to make it more amiable to existing code bases. Examples include GNU GCC extensions, ETSI fractional libraries, and multiple heap support.

A compiler's first job is to produce correct code, so there are occasions when the compiler must take a conservative approach to a code sequence when a more aggressive approach should have been taken if certain constraints were guaranteed by the programmer. The VisualDSP++ compiler supports a broad range of pragma that allows the programmer to better exploit the compiler while maintaining C language neutrality. Just as important, the compiler has the ability to feed back advisory information to the programmer, offering further improvements to a code sequence should the programmer be able to make certain guarantees about it. This information is displayed seamlessly in the VisualDSP++ main editor window. This "lifts the veil" off the "black box" that compilers are often, and accurately, accused of being.

VisualDSP++
Integrated Development Environment

```
#include <fract.h>
fract32 sp (fract16* a, fract16* b)
{
    int i;
    fract32 sum = 0;

    #pragma all_aligned
    for ( i = 0; i < 100; ++i )
    {
```
[Info] This loop executes 2 iterations of the original loop in estimated 1 cycles.
[Info] Loop was vectorized by a factor of 2
[Advice] Consider using pragma extra_loop_loads for this loop.
```
    }

    return sum;
}
```

Backing the compiler is a powerful assembler and linker technology. Analog Devices processors are noted for their intuitive algebraic assembly language syntax, and the VisualDSP++ assembler extends that ease of use with the ability to import C header files, allowing for symbolic references into arbitrarily complex C data structures. Binary data can be "included" directly into assembly source files, creating an easy way to add blocks of static data (such as audio samples and bitmaps) to an application. The VisualDSP++ linker is fully multicore and multiprocessor (MP) aware, allowing for the creation of cross-linked, multiexecutable applications in a single pass. Other powerful capabilities of the linker include dead code and data elimination, code and data overlays, section spilling (i.e., automatic overflow from internal to external memory), and automatic short-to-long call expansion.

Leverage Proven Application Infrastructure

VisualDSP++ goes beyond robust code generation tools, providing considerable application infrastructure and "middleware" out-of-the-box to speed application development. The VisualDSP++ Kernel (VDK) is a robust, royalty-free real-time operating system (RTOS) kernel. It provides essential kernel features in a minimal footprint. Features include a fully pre-emptive scheduler (time slicing and cooperative scheduling are also supported), thread creation, semaphores, interrupt management, inter-thread messaging, events, and memory management (memory pools and multiple heaps). In MP environments, MP messaging is also provided. Configuration of these elements is done graphically, with code wizards to speed the creation of new threads and interrupt handlers. VDK has been available for multiple releases of VisualDSP++ and is now a key component of products shipping from a number of high volume vendors. Several commercial RTOSs are also available from select Analog Devices third parties.

Blackfin processors can take advantage of the system service library (SSL), which provides consistent, easy C language access to Blackfin features such as the interrupt manager, direct memory access (DMA), and power management units. Clock frequency and voltage can be changed easily at run time through a set of simple APIs. Interrupt handling can be "live," fired at the time of the event, or "deferred" to a later time of the application's choosing. A device manager integrates device drivers for on- and off-chip peripherals. VisualDSP++ includes ever expanding device driver support for all on-chip peripherals and off-chip devices found on Analog Devices EZ-KIT Lite and EZ-Extender products. The SSL is OS-neutral and can be run as a standalone or in conjunction with an RTOS.

Built upon the system service library, the file system service (FSS) provides a portable and extensible means of accessing mass storage media from the Blackfin processor. Support for the ADSP-BF548 EZ-KIT Lite development board is provided with VisualDSP++ 5.0 for FAT file systems on the attached hard disk drive, supplied SD card, and USB flash.

As embedded applications become increasingly part of the "connected world," the ability to rapidly add reliable Ethernet or USB connectivity to an application can often make or break a development schedule. For Blackfin processors, VisualDSP++ includes a tuned port of the open-source LwIP TCP/IP stack. An example application showcasing an embedded Web server is among the highlights of this support. For Blackfin processors and SHARC processors, USB 2.0 device connectivity is provided. Bulk and asynchronous transfer modes are supported out of the box, with USB-IF logo certified embedded and host applications provided with full source code.
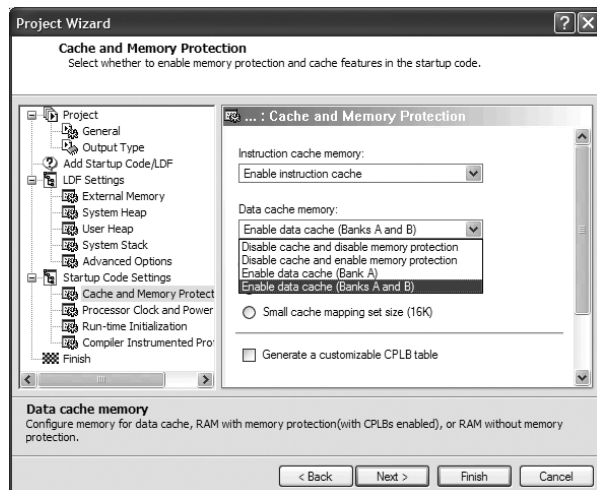
Source code generation.

Wrapping all of these powerful tools and libraries is the VisualDSP++ state-of-the-art integrated development and debugging environment (IDDE). The IDDE includes full-featured editing and project management tools, with incremental builds, multiple build configurations ("debug" and "release," for example), syntax-coloring editor, and many other code editing features. Makefiles can be imported and exported freely. For Blackfin processors, many application attributes can be configured graphically, enabling point-and-click access to SDRAM setup, stack and heap placement, power management, clock speed, cache setup, and more.

Debug and Tune Your Application with Ease

The ability to develop a high performance application is often gated by the visibility into the running system that your debugger provides. VisualDSP++ excels in this regard, with best-in-class debugging and inspection support. Robust fundamental C language source debugging (source level stepping and breakpoints, stack unwinds, local variable and C expression support, memory and register windows) serves as a foundation upon which multiple innovative and unique tools rest.

VisualDSP++
## *Integrated Development Environment*

VisualDSP++ supports a variety of debugging "targets." Most common is a JTAG connection to an EZ-KIT Lite board or to a custom target board by means of Analog Devices emulator products. However, there will be occasions where closer inspection in a simulated environment may be required. VisualDSP++ provides core cycle-accurate simulators, allowing inspection of every nuance of activity within the processor, including visualization of the processor's pipeline and cache. These simulators are robust and highly accurate, so much so that they are used by Analog Devices' own silicon designers for validation. A second simulator is available to Blackfin processor users—a high speed functional simulator. Using proprietary just-in-time (JIT) technology, the simulators have the ability to simulate millions of cycles per second on the most modest of host PCs. Effectively, this means that what used to be an overnight run is now a 10-minute coffee break, and what was once a coffee break is now a near instantaneous simulation.

As many of the most performance-demanding applications process a signal of some sort, comprehensive memory plotting is a cornerstone of VisualDSP++ debugger support. VisualDSP++ provides multiple views, from basic (line plots) to sophisticated (eye diagrams and waterfalls), to pinpoint anomalous data sequences in your application. Image viewing in a number of data formats is also available.
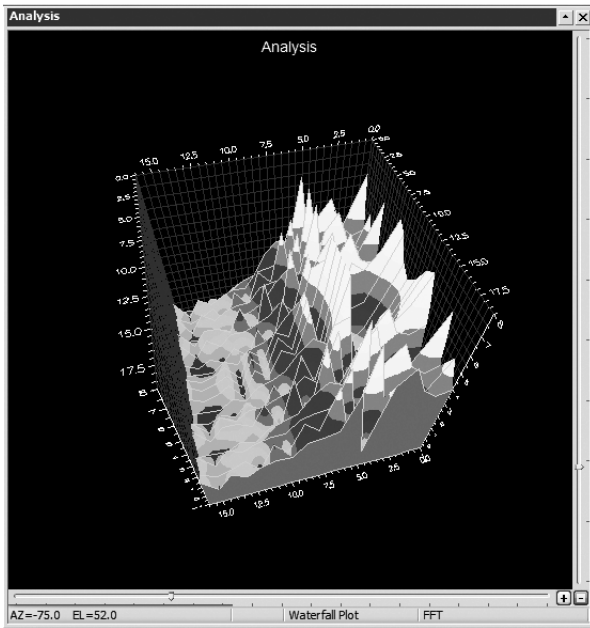
Comprehensive memory plotting.

Users of the VDK get unparalleled visibility into the internals of the kernel. Status on a per-thread basis is available, as is a comprehensive pictorial history of kernel events and CPU loading. Thread changes, posted and pended semaphores, and other kernel events are captured in this display.
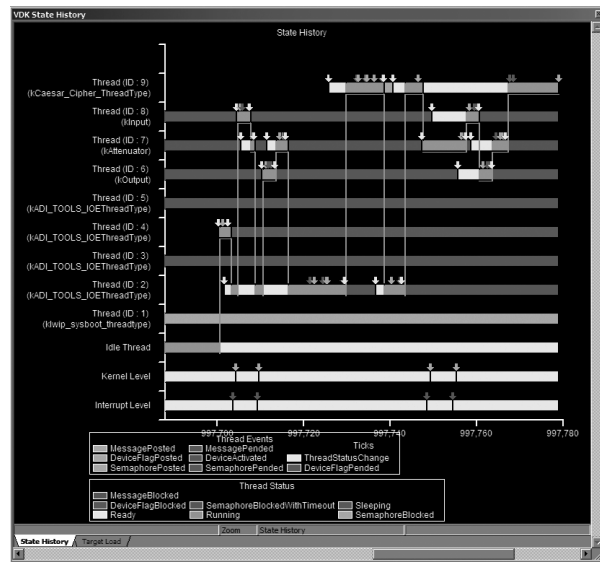
Kernel event history.

For Blackfin processors and SHARC processors, inspection, or even application stimulation, from the debugger at run time is possible through the use of the processor's background telemetry channel (BTC). BTC allows for an arbitrary number of communication channels to be established between the host debugger and application. Channels may go in either direction, so BTC can be used to read and write data as the processor runs. Scalar values or entire arrays may be serviced by a channel. Arrays read from the target can even be plotted in real time.

MP users get the same compelling set of debugging features across all processors, unified into a single debugging interface. Individual windows can be made to "float" their focus to whichever processor currently is the debugger's focus, or they can be "pinned" to a specific processor so their contents do not follow the debugger's focus. To further aid MP debug, synchronous run, step, halt, and reset are also provided.

The Analog Devices patented statistical profiler offers unprecedented and unique visibility into a running application. Operating completely nonintrusively to the application, the application is polled thousands of times per second, and a statistical view of where an application is spending the majority of its time is quickly assembled. This tool can be used to easily inspect an application for unexpected hotspots (suggesting the need to move a key routine from external to internal memory, for example). Simulator targets provide a completely linear profiling view. For Blackfin processors, traditional instrumented profiling is also available.

Going even further, the VisualDSP++ compiler is able to act upon profiling information. Profile-guided optimization (PGO) is a technique that allows the compiler to instrument an application, run the application, and then make a second-pass compilation, exploiting the information that was gathered during the run of the application. This gives the compiler unique insight on a block-by-block basis, allowing it to optimize with a level of granularity that is not possible with a tool that operates only a file-by-file basis.

VisualDSP++
Integrated Development Environment

Integrate into Your Existing Environment

A development tool suite is always a part of an organization's larger software engineering environment. VisualDSP++ has been designed to operate in a larger environment.

Since an embedded engineer is often developing on a new platform while maintaining existing products that were likely developed with an earlier version of the tools, VisualDSP++ can be installed discretely an arbitrary number of times at a variety of release levels, allowing engineering to easily switch between current and legacy versions of VisualDSP++.

To better integrate to source code control (SCC) systems, VisualDSP++ is able to connect to any SCC provider that supports the Microsoft Common Source Code Control (MCSCC) interface. This interface is supported by all leading SCC vendors. VisualDSP++ goes one step further by supporting the control of VisualDSP++ itself within a source code control system.

The ability to robustly test an embedded application is enabled through a comprehensive automation application programmers interface (API). Using Microsoft's language-neutral automation technology, nearly every feature of the graphical environment is available to script authors.

Applications can be rebuilt, downloaded, and run from a simple script executed from the command-line or from within a custom test harness framework. The automation API is supported by C++ and VBScript examples for all API calls, though any automation-aware language can be used.

For prototype runs and/or small volume deployment, an Analog Devices emulator can be used to flash a program onto your custom system. Accessible through the automation API, the flash programmer can be scripted, making it possible to develop a turnkey user interface for use by a production floor technician or other individual not familiar with VisualDSP++. Device drivers are provided for all flash devices found on EZ-KIT Lite products, and these drivers are easily adjusted to support an arbitrary flash device.

The standalone flash programmer enables the development engineer to script or automate this process with a license-free tool, allowing the manufacturing technician to repeatedly program any number of boards prior to major production.

To download a test drive, visit *www.analog.com/testdrive.*

Development Tools
Extended Development Tools Products

In addition to CROSSCORE development tools, there are a variety of starter kits, hardware, and software available.

Starter Kit—provides everything needed to get started on an application. Starter kits contain a Blackfin EZ-KIT Lite, EZ-Extender daughter board(s), and the Software Development Kit (SDK), which contains sample code, "how to" documents, and various encoders/decoders that make getting started on an application easy and shortens the learning curve.

Software Development Kits (SDK)—contains example software, source code, device drivers, algorithms, utilities information, and application notes that allow you to develop processor applications. The software can be used as a framework, or as examples of how to use certain aspects and peripherals, in conjunction with an ADI processor. The SDK is included in the starter kits and is also available for free download, provided you have the required hardware, at *www.analog.com/SDK/downloads*.

Multimedia Starter Kit—provides everything you need to get started on a multimedia application. Using a Blackfin EZ-KIT Lite and EZ-Extenders daughter board(s) to perform multimedia related tasks, learn how to render/capture video and audio streams using various off the shelf multimedia devices. As well, the SDK contains source code, "how to" documents, and various encoders/decoders that make getting started easy and shorten the learning curve.

Media Player Starter Kit—provides everything you need to get started on a media player application using a Blackfin EZ-KIT Lite and included software to perform audio and graphic related tasks. Learn how to render audio contents and images to the on-board peripherals from the on-board storage devices such as the hard drive and memory sticks. The SDK contains source code, "how to" documents, and various decoders that make getting started easy and shorten the learning curve.

μClinux—is an open-source OS that has gained significant attention and popularity over the past few years. There are several advantages to having open-source tools available for the Blackfin processor: source code availability, royalty-free licenses, reliability, community support, tools availability, networking support, portability, and an extensive application base. Developers have the opportunity to develop even the most demanding feature-rich applications in a very short time frame and can leverage the work of others in the community. The μClinux kernel and GNU toolchain have been ported to the Blackfin processor and are both available for download from the μClinux website. This website (*www.blackfin.uclinux.org*) is the central repository for all open-source Blackfin projects. Examples of current Blackfin projects are: GNU Toolchain for Blackfin (gcc 3.x), Uboot for the Blackfin Processor, CoLinux Port of Blackfin Tools, μClinux for Blackfin Documentation, JTAG Tools for Blackfin, Networked Audio Media Node, and Networked Oscilloscope.

One of the board support packages is the ADSP-BF537 STAMP μClinux Kernel board support package (BSP). The STAMP board has been specifically designed to support the development and porting of open-source μClinux applications and includes the full complement of memory along with serial and network interfaces. A variety of daughter cards that plug into this board are also available. Go to *www.blackfin.uclinux.org* for the most current open-source hardware and software information for the Blackfin processor.

CROSSCORE Development Tools Selection Table

Processor	Hardware	Emulator	VisualDSP++ Development Software	Additional Software Available
Blackfin Processors				
ADSP-BF592	ADZS-BF592-EZLITE	ADZS-ICE-100B ADZS-USB-ICE ADZS-HPUSB-ICE	VDSP-BLKFN-PC-TEST VDSP-BLKFN-PC-FULL VDSP-BLKFN-PCFLOAT VDSP-BLKFN-PCFLT-5	
ADSP-BF504 ADSP-BF504F ADSP-BF506F	ADZS-BF506F-EZLITE			
ADSP-BF512/ADSP-BF512F ADSP-BF514/ADSP-BF514F ADSP-BF516/ADSP-BF516F ADSP-BF518/ADSP-BF518F	ADZS-BF518F-EZLITE ADZS-BF518F-EZBRD ADZS-DBGAGENT-BRD ADZS-BFLLCD-EZEXT ADZS-BLUET-EZEXT ADZS-BFSHUSB-EZEXT			Software Development Kit (SDK) (ADSP-BF527, ADSP-BF533, ADSP-BF537, ADSP-BF548, ADSP-BF561 only)
ADSP-BF522/ADSP-BF522C ADSP-BF524/ADSP-BF524C ADSP-BF526/ADSP-BF526C	ADZS-BF526-EZLITE ADZS-BF526-EZBRD ADZS-BFLLCD-EZEXT ADZS-DBGAGENT-BRD ADZS-BLUET-EZEXT ADZS-BFSHUSB-EZEXT			Mathworks (ADSP-BF531, ADSP-BF532, ADSP-BF533, ADSP-BF534, ADSP-BF536, ADSP-BF537, ADSP-BF538, and ADSP-BF539 only)
ADSP-BF523/ADSP-BF523C ADSP-BF525/ADSP-BF525C ADSP-BF527/ADSP-BF527C	ADZS-BF527-EZLITE ADZS-BF527-MPSKIT ADZS-BFAV-EZEXT ADZS-BFFPGA-EZEXT			µClinux Kernel + GNU Software (All parts except the ADSP-BF535 and ADSP-BF50x family)
ADSP-BF531 ADSP-BF532 ADSP-BF533	ADZS-BF533-EZLITE ADZS-BF-EZEXT-1 ADZS-BFAV-EZEXT ADZS-USBLAN-EZEXT ADZS-BFAUDIO-EZEXT ADZS-BFFPGA-EZEXT ADZS-BF533-MMSKIT			Microsoft®.Net (Available on ADSP-BF527 only)
ADSP-BF535	—			
ADSP-BF534 ADSP-BF536 ADSP-BF537	ADZS-BF537-EZLITE ADZS-BFAV-EZEXT ADZS-BLUET-EZEXT ADZS-USBLAN-EZEXT ADZS-BFAUDIO-EZEXT ADZS-BFFPGA-EZEXT ADZS-BF537-STAMP ADZS-BFLLCD-EZEXT			
ADSP-BF538/ADSP-BF538F	ADZS-BF538F-EZLITE ADZS-BFLLCD-EZEXT			
ADSP-BF542 ADSP-BF544 ADSP-BF547 ADSP-BF548	ADZS-BF548-EZLITE ADZS-BF548-MPSKIT ADZS-BLUET-EZEXT ADZS-BFAV-EZEXT ADZS-BFFPGA-EZEXT ADZS-BFLLCD-EZEXT			
ADSP-BF561	ADZS-BF561-EZLITE ADZS-BF561-MMSKIT			
SHARC Processors				
ADSP-21160M ADSP-21160N	—	ADZS-USB-ICE ADZS-HPUSB-ICE	VDSP-SHARC-PC-TEST VDSP-SHARC-PC-FULL VDSP-SHARC-PCFLOAT VDSP-SHARC-PCFLT-5	Mathworks (ADSP-21363, ADSP-21364, ADSP-21366, ADSP-21367, ADSP-21368, and ADSP-21369 only)
ADSP-21161N	—			
ADSP-21261 ADSP-21262 ADSP-21266	ADZS-21262-EZLITE ADZS-21262-1-EZEXT ADZS-SHRCUSB-EZEXT			
ADSP-21363 ADSP-21364 ADSP-21366	ADZS-21364-EZLITE ADZS-SHRCUSB-EZEXT			
ADSP-21368 ADSP-21369	ADZS-21369-EZLITE ADZS-SHRCUSB-EZEXT			
ADSP-21371 ADSP-21375	ADZS-21371-EZLITE ADZS-21375-EZLITE			
ADSP-21467 ADSP-21469	ADZS-21469-EZLITE ADZS-21469-EZBRD ADZS-DBAGENT-BRD ADZS-SHAUDIO-EZEXT ADZS-BFSHUSB-EZEXT			
ADSP-21478 ADSP-21479	ADZS-21479-EZLITE ADZS-21479-EZBRD ADZS-DBAGENT-BRD ADZS-BFSHUSB-EZEXT			
ADSP-21483 ADSP-21486 ADSP-21487 ADSP-21488 ADSP-21489	ADZS-21489-EZLITE ADZS-21489-EZBRD ADZS-DBAGENT-BRD ADZS-BFSHUSB-EZEXT			
TigerSHARC Processors				
ADSP-TS101 ADSP-TS201 ADSP-TS202 ADSP-TS203	ADZS-TS201S-EZLITE	ADZS-USB-ICE ADZS-HPUSB-ICE	VDSP-TS-PC-TEST VDSP-TS-PC-FULL VDSP-TS-PCFLOAT VDSP-TS-PCFLT-5	Mathworks (Not available on the ADSP-TS101)

Software Modules for Blackfin and SHARC Processors

Overview

Analog Devices (ADI) software modules are a series of popular audio and video algorithms for Blackfin processor-based designs and a series of SHARC processors. The highly optimized software modules allow you to quickly and easily incorporate these multimedia functions, providing a fast development path to the end product. The software modules feature a consistent API to ensure rapid integration of multiple software algorithms.

Developed internally by ADI, these software module implementations are provided free to Blackfin and SHARC processor software programmers. New and revised modules and their supported processors are added frequently. For the latest information on software modules go to *www.analog.com/BlackfinModules* and *www.analog.com/SHARCModules*.

Hardware Requirements

The software modules run on ADI EZ-KIT Lite evaluation boards and EZ-Extender daughter boards or on custom boards with supported processors.

Availability and Licensing

Each module supports ADI Blackfin and SHARC processors and is a licensed product that is available in object code format.

Licensing restrictions for Dolby, DTS, and Microsoft

The customer must be a licensee for Dolby,® DTS,® SRS,® or Microsoft® before production code can be shipped for that particular algorithm. Dolby, DTS, SRS and Microsoft modules have been certified on specific processors.

Worldwide Support

Each software module includes a detailed product reference guide and demonstration code to get you started. Online information for each module is available on ADI's website, *www.analog.com/BlackfinModules* and *www.analog.com/SHARCModules*. Additional support for designers and programmers is available by visiting *www.analog.com/support*. Support for system integration is available through ADI third parties.

Features

- Free implementation of multimedia and other popular algorithms
- Most available as production downloadable code from the Web
- Modules developed directly by Analog Devices
- Highly optimized—coded by ADI processor experts
- Consistent API (application programming interface) and framework across all modules
- Demonstration applications provided
- Uses ADI development tools
- Runs on the latest revision of VisualDSP++
- Support for Blackfin and SHARC processors

Each Software Module Includes

- Library module with a standard C-callable API consistent with other code modules
- Reference C source code interface routine that calls the code as a single library module
- Demonstration software for execution on ADI evaluation boards
- Documentation, including application notes and detailed developers guides

Software Modules for Blackfin and SHARC Processors

Blackfin Processor Software Modules

Software	Type
Adaptive Jitter Buffer	Telephony/VoIP
Asynchronous Sample Rate Converter (ASRC)	Audio Postdecoder
Audio Mixer	Telephony/VoIP
Bit Stream Detector (for S/PDIF)	Audio Preprocessor
Blackfin Image Processing Toolbox	Image/Video Processing Primitives
Blackfin 2D Graphics Library (BF2DGL)	Graphics Engine
Dolby Digital (AC-3) 5.1 Decoder	Audio Decoders and Postdecoders
Dolby Digital (AC-3) Consumer Encoder	Audio Encoders
Dolby Digital EX Decoder	Audio Decoder
Dolby Headphone v2	Audio Decoders and Postdecoders
Dolby Pro Logic IIx	Audio Decoders and Postdecoders
Dolby Virtual Speaker (DVS)	Audio Decoders and Postdecoders
DTS 5.1 Decoder	Audio Decoders and Postdecoders
DTS Neo:6	Audio Decoders and Postdecoders
Dual Tone Multifrequency (DTMF) Decoder	Telephony/VoIP
Dual Tone Multifrequency (DTMF) Generator	Telephony/VoIP
Enhanced Video Post Processing (eVPP)	Video Postprocessor
G.711 Appendix I Voice Codec with PLC	Voice Codec
G.723.1A Voice Codec	Voice Codec
G.729AB Voice Codec	Voice Codec
H.264 BP Decoder	Video/Imaging Decoder
H.264 BP Encoder	Video Encoder
H.264 BP/MP Encoder	Video Encoder
JPEG Decoder	Imaging Decoder
JPEG Encoder	Imaging Encoder
MP3 Decoder (with Layer 1 and 2 support)	Audio Decoders and Postdecoders
MP3 Encoder	Audio Encoder
MPEG-2 Video Decoder	Video/Imaging Decoder
MPEG-4 AAC-BSAC Decoder	Audio Decoders and Postdecoders
MPEG-4 AAC-LC Decoder	Audio Decoder
MPEG-4 HE-AAC v2 Decoder (with DAB+ and DRM support)	Audio Decoders and Postdecoders
MPEG-4 HE-AAC v2 Encoder	Audio Encoders
MPEG-4 SP/ASP Decoder Library	Audio Decoders and Postdecoders
MPEG-4 Simple Profile and Advanced Simple Profile Video Encoder	Video Encoder
Multiband Graphic Equalizer	Audio Postdecoder
Ogg Vorbis Decoder	Audio Decoder
RTP/RTCP	Telephony/VoIP
Signal Tone Detector with Modem/Fax Passthrough	Telephony/VoIP
Signal Tone Generator	Telephony/VoIP
Video Analytics Toolbox	Video/Imaging Postprocessors
Windows Media Audio (WMA9) Standard Decoder	Audio Decoders and Postdecoders
Windows Media Audio (WMA9) Standard Encoder	Audio Encoders
Windows Media Video (WMV9) Standard Decoder	Video/Imaging Decoder
MPEG-2 Video Encoder	Video Encoders
Multimedia Format Processing Library	AV Format Parser
WAV PCM Utilities	Audio Decoders and Post Decoders

SHARC Processor Software Modules

Software	Type
Asynchronous Sample Rate Converter (ASRC)	Audio Postdecoders
Dolby Advanced Fader	Audio Decoders and Postdecoders
Dolby Intelligent Mixer (eMix)	Audio Decoders and Postdecoders
Dolby Digital (AC-3) 5.1 Decoder	Audio Decoders and Postdecoders
Dolby Digital EX Decoder	Audio Decoder
Dolby Headphone (DH) v2	Audio Decoders and Postdecoders
Dolby Pro Logic IIx	Audio Decoders and Postdecoders
Dolby Virtual Speaker	Audio Decoders and Postdecoders
DTS 5.1 Decoder	Audio Decoders and Postdecoders
DTS Neo:6 Matrix Decoder	Audio Decoders and Postdecoders
Dolby® Volume	Audio Decoders and Post Decoders
MPEG-4 AAC-LC Decoder	Audio Decoder
Neural Surround Decoder	Audio Decoders and Post Decoders

New modules are frequently being added.
Visit *www.analog.com/BlackfinModules* and
www.analog.com/SHARCModules for the latest listing.

Additional Support

Third-Party Developers Program for Embedded Processor and DSP Applications`

Find a Third Party to Help You Get Your Design to Market Faster

Analog Devices Third Party Developers network consists of companies all over the world that provide hardware products, software products, algorithms, and design services for a wide variety of applications and markets.

The third party search on our website allows you to quickly find the third parties that offer services for our Embedded Processors and DSPs. The interface allows you to easily filter our third party network by ADI processor(s) supported, offerings, regions supported, and markets and applications supported. You can also perform a keyword search of all the third party listings.

Visit the new Embedded Processing and DSP Third Party Search at *www.analog.com/3rdparty*.

Become an Analog Devices Third Party Developer at *www.analog.com/join-thirdpartynetwork*.

Platforms and Reference Designs

Platforms and reference designs help jump-start your design. They include comprehensive software suites with documented APIs running on application-specific evaluation boards. The easy to use APIs enable customization and control of core system functions, letting you focus on adding value through product differentiation. For more information on Analog Devices platforms, reference designs, and third-party reference designs, visit *www.analog.com/software.*

## EngineerZone—A Technical Support Forum from Analog Devices

Where DSP Engineers Go for the Right Answers

EngineerZone is a new online technical support forum that provides direct access to DSP technical support engineers.

Features

- Search FAQs and technical information to get quick answers to your embedded processing and DSP design questions
- Connect with other DSP developers who face similar design challenges
- Share knowledge and collaborate with the ADI support team and your peers in this open forum

Join the forum at *EZ.analog.com.*
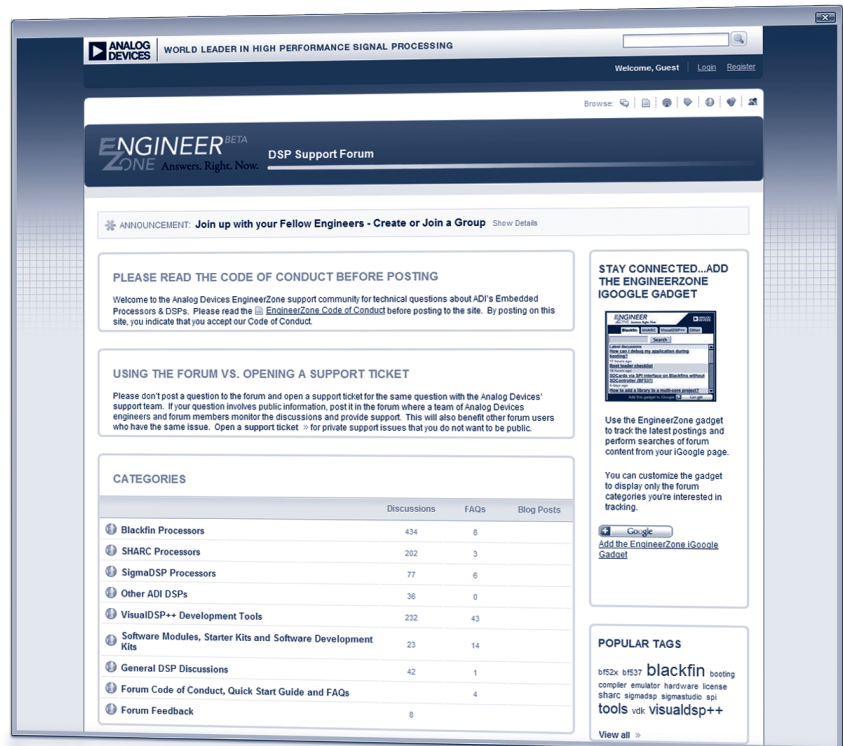
Benchmarks
Comparing Processors

To truly assess a processor's performance, you have to look beyond MHz, MIPS, or MFLOPS. There are many attributes that may be more accurate predictors of real-time signal processing performance.

Circular Buffers

Circular buffers allow a region of memory to be continually accessed without explicit program interaction. The buffer uses a pointer that automatically resets to the beginning of the buffer (wraparound) if the pointer is advanced beyond the last location in the buffer. Circular buffers are a key feature of DSP routines. Multiple buffers are used in the same routine to store filter coefficients and implement a delay line of input samples. Performance suffers if the DSP core has to perform pointer calculations along with the calculations for the routine. Performance also suffers if the DSP core only supports one circular buffer and must save and restore address registers to implement multiple buffers.

Analog Devices processors have hardware support for multiple circular buffers, eliminating processor overhead for address calculations.

DMA Channels/Nonintrusive DMA

The DMA (direct memory access) channels transfer data between an external source and the processors' on-chip memory. With DMA channels, data transfers occur without the core processor having to execute data movement instructions. For example, the overhead clock cycles used to move data for an FFT can add a significant amount of time to overall algorithm execution. With multiple DMA channels available, all data transfers happen without core involvement, eliminating any overhead clock cycles.

One of the strengths of Analog Devices processor architecture is that these DMAs do not interfere with the core operation. This capability is referred to as nonintrusive or zero-overhead DMA.

Interrupt Latency

Interrupt latency is a measure of how quickly a processor responds to an interrupt. Quick response is important, especially in real-time processing. For example, an interrupt that might indicate the availability of data is only available for a finite amount of time; therefore, fast response is critical, or the data will be lost.

Analog Devices products feature fast interrupt response time for quick execution of interrupt service routines.

Multiprocessing Support

Even with the powerful DSPs available today, there are times when the DSP task for a given system does not fit into a single processor. Examples of such applications include sonar, radar, medical imaging, audio mixers, etc. In these cases, the ability to connect multiple processors in a system without any glue logic greatly simplifies the implementation.

Analog Devices offers SHARC and TigerSHARC processors with specialized hardware for glueless multiprocessing.

On-Chip Memory/On-Chip SRAM Size

The amount of on-chip memory available can greatly impact system performance, cost, size, power consumption, and complexity. Any time the DSP core accesses external memory, performance can suffer. Off-chip memory often requires the core to wait additional cycles. In contrast, the DSP core can access on-chip memory at the same rate as its instruction rate. Supplemental memory adds extra components to the system, which increases cost, power consumption, and complexity.

ADI processors have on-chip memories that often eliminate the need for external memory in a system. Furthermore, the memory is configurable for data-word size, code word size, and storage size. This allows designers to tailor the memory to meet the algorithm requirements.

TDM Mode

TDM (time division multiplexed) mode refers to time division multiplexing, which is a common mode for transferring serial data. In telecommunications applications, T1 and E1 lines use TDM. TDM allows multiple serial devices to send and receive information using the same physical connection. TDM also allows communication between multiple processors.

All ADI products support TDM mode in the serial ports.

Zero-Overhead Looping

The code for most DSP routines falls naturally into a set of nested loops. Without the support for zero-overhead looping, the DSP core must spend cycles calculating the loop termination values, in addition to the cycles used to process the algorithm's computations. Without zero-overhead looping, performance degrades.

Analog Devices offers 16-bit fixed-point and 32-bit fixed- and floating-point processors with zero-overhead, nestable looping to save instruction cycles.

ADI Processor Benchmarks[1]

	Cycle Count	Execution Time @ 600 MHz
Blackfin Processor		
Block FIR Filter	(x/2)(2 + h)	
Biquad IIR Filter (4 Coeff)	2.5bq + 3.5	
Complex FIR Filter	2h + 2	
Delayed LMS Filter	1.5h + 4.5	
1024-Point Complex FFT (Prescaled)	11,559	19.3 μs
256-Point Complex FFT (Out of Place)	2324	3.87 μs
Max Search	0.5N	
Max Index Search	0.5N	

	ADSP-21160N ADSP-21161N	ADSP-2126x	ADSP-2136x	ADSP-21371 ADSP-21375	ADSP-2146x
SHARC Processor (SIMD)					
Clock Speed	100 MHz	200 MHz	400 MHz	266 MHz	450 MHz
Instruction Cycle Time	10 ns	5 ns	2.5 ns	3.75 ns	2.22 ns
MFLOPS Sustained	400 MFLOPS	800 MFLOPS	1600 MFLOPS	1064 MFLOPS	1800 MFLOPS
Peak	600 MFLOPS	1200 MFLOPS	2400 MFLOPS	1596 MFLOPS	2700 MFLOPS
MOPS (32-Bit, Fixed-Point) Sustained	400 MFLOPS	800 MFLOPS	1600 MFLOPS	1064 MFLOPS	1800 MFLOPS
Peak	600 MFLOPS	1200 MFLOPS	2400 MFLOPS	1596 MFLOPS	2700 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	92 μs	46 μs	23 μs	34.5 μs	20.44 μs
FIR Filter (per Tap)	5 ns	2.5 ns	1.25 ns	1.88 ns	1.11 ns
IIR Filter (per Biquad)	20 ns	10 ns	5.0 ns	7.5 ns	4.43 ns
Matrix Multiply (3 × 3) × (3 × 1)	45 ns	22.5 ns	11.25 ns	16.91 ns	10.00 ns
(4 × 4) × (4 × 1)	80 ns	40 ns	20.0 ns	30.07 ns	17.78 ns
Divide (y/x)	30 ns	15 ns	7.5 ns	11.27 ns	6.67 ns
Inverse Square Root	45 ns	22.5 ns	11.25 ns	16.91 ns	10.00 ns

	Cycle Count	Execution Time @ 600 MHz
TigerSHARC Processor		
256-Point Radix 2 Complex FFT (16-Bit)	525	0.875 μs
1k Point Complex FFT[2] (Radix 2) (32-Bit)	9384	15.64 μs
64k Point Complex FFT[2] (Radix 2) (32-Bit)	1,397,544	2.33 ms
FIR Filter (per Real Tap) (32-Bit)	0.5	0.83 ns
[8 × 8][8 × 8] Matrix Multiply (Complex, Floating-Point)	1399	2.3 μs

NOTES
[1] Benchmarks are for best data conditions.
[2] Cache preloaded.

h = number of taps.
bq = number of biquads.
x = number of samples.

ADI Processor Benchmarks

EEMBC Blackfin Comparison

EEMBC® benchmarks represent out-of-the-box performance for a typical suite of consumer applications. For more information, see *www.eembc.com*.

Blackfin Controller Performance

Processor	Blackfin	ARM1136JF-S	ARM926EJ-S
Product	*ADSP-BF533*	*i.MX31*	*i.MX21*
Clock Frequency (MHz)	594	532	266
Certified on Hardware?	*Yes*	*Yes*	*Yes*
EEMBC Networking 2.0[1]			
IPmark[2]	45	50.4	24.4
TCPmark[2]	117	68.5	29.2[3]
EEMBC Autobench 1.1[1]			
Automark[2]	183.1	126.6	29.6
EEMBC ConsumerBench1.1[1]			
Consumermark[2]	54.9	26.6	13.7
EEMBC AOBench1.1[1]			
AOmark[2]	352	341	152
EEMBC TeleBench1.1[1]			
Telemark[2]	11.7	6.1	2.5
EEMBC DENBench1.0[1]			
MPEG Decodemark[2]	337	231	112
MPEG Encodemark[2]	392	243	100
Cryptomark[2]	257	219	104
Imagemark[2]	352	315	154
DENmark[2]	57.5	45.5	21.6
EEMBC Geometric Mean	138.7	99.3	42.6

NOTES

[1] Out-of-the-box category.

[2] Iterations per second (bigger is better).

[3] i.MX21 TCPmark contains an estimate for one subtest whose result is filed n/a at EEMBC. (Estimate is ½ i.MX31 performance.)

EEMBC is a registered trademark of the Embedded Microprocessor Benchmark Consortium.
For more information and scores, go to *www.eembc.org*.

Blackfin Processor Family
High Performance, Low Power Processing Leadership

Blackfin processors are a new breed of embedded media processors, designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. Blackfin processors combine a 32-bit RISC-like instruction set and dual 16-bit multiply accumulate (MAC) signal processing functionality with the ease-of-use attributes found in general-purpose microcontrollers. Blackfin processors perform equally well in both signal processing and control processing applications, in many cases deleting the requirement for separate heterogeneous processors. This capability greatly simplifies both the hardware and software design implementation tasks.

Blackfin processors offer performance up to 600 MHz/1200 MMACS in single-core products. Symmetric, multiprocessor members of the Blackfin family extend this performance to over 3000 MMACS. The family offers the lowest power consumption—as low as 0.15 mW/MMAC at 0.8 V. The combination of high performance and low power is essential in meeting the needs of today and future signal processing applications, including broadband wireless, audio-/video-capable Internet appliances, and mobile communications.

All Blackfin processors offer fundamental benefits to the system designer, including:

- High performance signal processing and efficient control processing capability
- Dynamic power management (DPM), enabling the system designer to tailor device power consumption to the end-system requirements
- Easy to use instruction set architecture and development tools suite that saves development time

High Performance Signal Processing

The Blackfin processor architecture employs numerous techniques to ensure that signal processing performance is maximized. These include a fully interlocked instruction pipeline, multiple parallel computational blocks, efficient DMA capability, and instruction set enhancements designed to accelerate video processing.
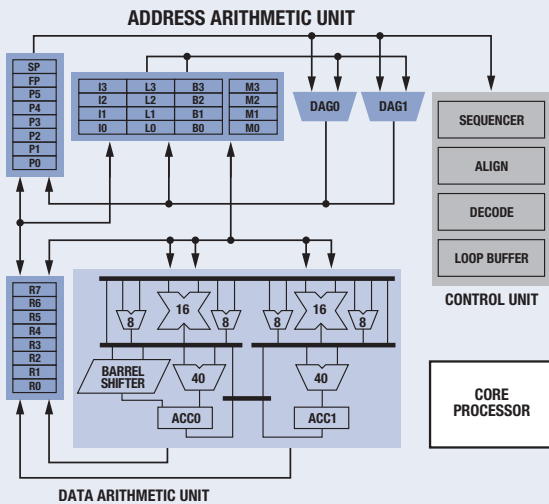
Efficient Control Processing

The Blackfin processor architecture also offers a variety of benefits most often seen in RISC control processors. These features include a hierarchical memory architecture, superior code density, and a variety of microcontroller-style peripherals, including a watchdog timer, a real-time clock, and an integrated SDRAM controller. All of these features provide the system designer with a great deal of design flexibility while minimizing end system costs.
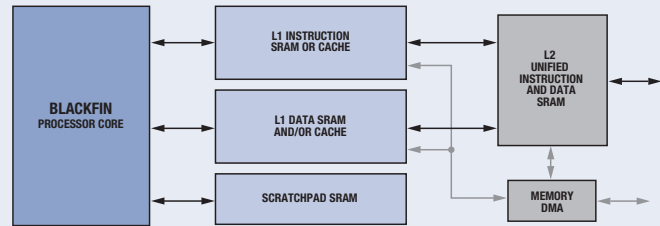
Dynamic Power Management

All Blackfin processors employ multiple power-saving techniques. Blackfin processors are based on a gated clock core design that selectively powers down functional units on an instruction-by-instruction basis. Blackfin processors also support multiple power-down modes for periods when little or no CPU activity is required. Last, and probably most importantly, Blackfin processors support a dynamic power management scheme whereby the operating frequency and voltage can be tailored to meet the performance requirements of the algorithm currently being executed. These transitions may occur continually under the control of an RTOS or user firmware. Some currently available products also offer on-chip core voltage regulation circuitry as well as operation to as low as 0.8 V and all are particularly well-suited for portable applications requiring extended battery life.

Easy to Use

A single Blackfin processor can be utilized in many applications previously requiring both a high performance signal processor and a separate efficient control processor. This benefit greatly reduces development time and costs, ultimately enabling end products to get to market sooner. Additionally, a single set of development tools can be used, which decreases the system designer's initial expenses and learning curve.

Blackfin Processor Family

Analog Devices' long-term commitment to the Blackfin processor means each subsequent generation of Blackfin-based designs will benefit from increases in speed, power efficiency, and cost reductions across a broad range for single and dual core processors.

The Blackfin processor family includes devices that target a wide range of applications in the consumer, automotive, industrial, instrumentation, and communications markets. To address these markets, the Blackfin processor family offers scalable performance from the 200 MHz ADSP-BF535 to the dual core 600 MHz ADSP-BF561 to the ADSP-BF52x with advanced peripherals to the low power ADSP-BF51x family with real-time Ethernet capabilities and the ADSP-BF50x with integrated flash and analog-to-digital converter. Future devices will further extend ADI's leadership in performance and power efficiency while maintaining code compatibility and providing the widest array of processor options for the most demanding convergent processing challenges.

Blackfin Processor Product Portfolio

Value → Highest Performance

	ADSP-BF592	ADSP-BF504 ADSP-BF504F ADSP-BF506F	ADSP-BF512	ADSP-BF514 ADSP-BF516 ADSP-BF518	ADSP-BF522 ADSP-BF524 ADSP-BF526	ADSP-BF523 ADSP-BF525 ADSP-BF527	ADSP-BF531 ADSP-BF532	ADSP-BF533	ADSP-BF534 ADSP-BF535 ADSP-BF536	ADSP-BF537	ADSP-BF538 ADSP-BF539	ADSP-BF542 ADSP-BF544 ADSP-BF547 ADSP-BF548	ADSP-BF561	Future
Low BOM Cost	●	●	●		●	●	●							
Baseline Connectivity	●	●	●		●	●	●	●					●	
System-Level Connectivity		●		●	●	●			●	●	●	●		●
Low Standby	●	●	●	●	●									●
Lockbox Security			●	●	●	●						●		●
System Integration (Flash, Mixed-Signal)		●	●	●	●	●					●			
600 MHz or Greater						●		●		●		●	●	●
Multicore													●	●

Blue product number indicates automotive grade is available.

Blackfin Processor Family Selection Table

Single Core

Part Number	Clock Speeds (MHz)	16-Bit Fixed-Point MMACS	On-Chip L1 Program (Bytes)	On-Chip L1 Data (Bytes)	Other Internal Memory (Bytes)	External Memory Type Supported	DMA (Channels)	Serial Ports	Other Ports/Features	Number of GPIOs	Timers	Core V$_{DDINT}$ (Max Speed)	External (I/O)	Total Core Power Typ (mW)[3]	Package[4,5]	Temperature Range (Nonautomotive Grade)	Temperature Range Automotive Grade (W)[2]	Price @ 1k ($U.S.)[6]	Availability
ADSP-BF592	400	800	32k SRAM	32k SRAM (+ 4k scratchpad)	64k L1 ROM	—	9	1 UART, 2 SPORTs, 2 SPIs, TWI	PPI/LCD, ROM libraries	Up to 32	4 GP, 3 PWM	1.4[7] (400 MHz) 1.3[7] (300 MHz)	1.8, 2.5, 3.3	127[7] (400 MHz) 86[7] (300 MHz)	9 mm × 9 mm, 0.5 mm 64-lead LFCSP	-40°C to +85°C, 0°C to +70°C	-40°C to +105°C, -40°C to +85°C	3.55[7]	Production
ADSP-BF592-2	200	400															—	1.99	
ADSP-BF504	400	800	16k SRAM/cache + 16k SRAM	16k SRAM/cache + 16k SRAM (+ 4k scratchpad)	—	—	14	2 UARTs, 2 SPORTs, 2 SPIs, TWI CAN	PPI/LCD, RSI/SDIO, 2 PWMs, 2 rotary encoders, ACM	Up to 35	8 GP, WD	1.4[7]	1.8, 2.5, 3.3	145[7]	12 mm × 12 mm, 0.5 mm 88-lead LFCSP	-40°C to +85°C, 0°C to +70°C	-40°C to +105°C, -40°C to +85°C	5.18[7]	Production
ADSP-BF504F	300	600			4M parallel flash							1.225[7]	3.3	84[7]			—	7.48[7]	
ADSP-BF504F	400	800										1.4[7]		145[7]				8.06[7]	
ADSP-BF506F	300	600							PPI/LCD, RSI/SDIO, 2 PWMs, 2 rotary encoders, ACM, 12-bit dual SAR ADC (12-channel)			1.225[7]	3.3	84[7]	14 mm × 14 mm, 0.4 mm 120-lead LQFP_EP	-40°C to +85°C, 0°C to +70°C	—	12.21[7]	Production
ADSP-BF506F	400	800										1.4[7]		145[7]				12.78[7]	
ADSP-BF512	300	600	16k SRAM/cache + 32k SRAM	32k SRAM/cache + 32k SRAM (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM	14	2 UARTs, 2 SPORTs, 2 SPIs, TWI	PPI/LCD, PWM, rotary encoder, Lockbox	Up to 40	8 GP, WD, RTC	1.225	1.8, 2.5, 3.3	84	12 mm × 12 mm, 0.8 mm, 168-ball CSP_BGA; 24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP	-40°C to +85°C, 0°C to +70°C	-40°C to +85°C	6.26	Production
ADSP-BF512	400	800										1.40		150			-40°C to +85°C	8.35	
ADSP-BF512F	400	800			512k SPI flash							1.40		150			—	9.73	
ADSP-BF514	300	600							PPI/LCD, Lockbox, ATAPI, RSI/SDIO, rotary encoder, PWM			1.225		84	12 mm × 12 mm, 0.8 mm, 168-ball CSP_BGA; 24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP	-40°C to +85°C, 0°C to +70°C	-40°C to +85°C	7.77	
ADSP-BF514	400	800										1.40		150			-40°C to +85°C	8.92	
ADSP-BF514F	400	800			512k SPI flash							1.40		150			—	10.31	
ADSP-BF516	300	600							Ethernet MAC, PPI/LCD, Lockbox, ATAPI, RSI/SDIO, rotary encoder, PWM			1.225		84	12 mm × 12 mm, 0.8 mm, 168-ball CSP_BGA; 24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP	-40°C to +85°C, 0°C to +70°C		8.92	
ADSP-BF516	400	800										1.40		150			—	10.08	
ADSP-BF516F	400	800			512k SPI flash							1.40		150				11.46	
ADSP-BF518	400	800			—				Ethernet MAC (IEEE 1588), PPI/LCD, Lockbox, ATAPI, RSI/SDIO, rotary encoder, PWM			1.40		150	12 mm × 12 mm, 0.8 mm, 168-ball CSP_BGA; 24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP	-40°C to +85°C	—	13.07	
ADSP-BF518F	400	800			512k SPI flash							1.40		150				14.45	
ADSP-BF522	300	600	16k SRAM/cache + 48k SRAM	32k SRAM/cache + 32k SRAM (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM, NAND flash	14	2 UARTs, 2 SPORTs, SPI, TWI	PPI/LCD, Lockbox, host DMA, rotary encoder	Up to 48	8 GP, WD, RTC	1.225	1.8, 2.5, 3.3	93	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA; 12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	-40°C to +85°C, 0°C to +70°C	—	8.18	Production
ADSP-BF522	400	800										1.40		158	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA; 12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	-40°C to +85°C, 0°C to +70°C		10.33	
ADSP-BF523	533	1066										1.15		166	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	-40°C to +85°C, 0°C to +70°C	—	13.46	Production
ADSP-BF523	600	1200										1.20		205	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	0°C to +70°C		16.99	
ADSP-BF524	300	600			—			USB 2.0 HS OTG, 2 UARTs, 2 SPORTs, SPI, TWI				1.225		93	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA; 12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	-40°C to +85°C, 0°C to +70°C	—	9.58	Production
ADSP-BF524	400	800										1.40		158	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA; 12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	-40°C to +85°C, 0°C to +70°C		12.03	

Single Core

Part Number	Clock Speeds (MHz)	16-Bit Fixed-Point MMACS	On-Chip L1 Program (Bytes)	On-Chip L1 Data (Bytes)	Other Internal Memory (Bytes)	External Memory Type Supported	DMA (Channels)	Serial Ports	Other Ports/Features	Number of GPIOs	Timers	Core V (Max Speed)	External (I/O)	Total Core Power Typ (mW)	Package	Temperature Range (Nonautomotive Grade)	Temperature Range Automotive Grade (W)	Price @ 1k ($U.S.)	Availability
ADSP-BF525	533	1066	16k SRAM/cache + 48k SRAM	32k SRAM/cache + 32k SRAM (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM, NAND Flash	14	USB 2.0 HS OTG, 2 UARTs, 2 SPORTs, SPI, TWI	PPI/LCD, Lockbox, host DMA, rotary encoder	Up to 48	8 GP, WD, RTC	1.15	1.8, 2.5, 3.3	166	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	−40°C to +85°C	15.17	Production
ADSP-BF525	600	1200										1.20		205	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C	—	18.71	Production
ADSP-BF526	300	600							Ethernet MAC, PPI/LCD, Lockbox, host DMA, rotary encoder			1.225		93	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C	—	10.76	Production
ADSP-BF526	400	800										1.40		158	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	—	13.82	Production
ADSP-BF527	533	1066										1.15		166	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	—	16.99	Production
ADSP-BF527	600	1200										1.20		205	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C	—	20.56	Production
ADSP-BF522C	300	600	16k SRAM/cache + 48k SRAM	32k SRAM/cache + 32k SRAM (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM, NAND flash	14	2 UARTs, 2 SPORTs, SPI, TWI	PPI/LCD, Lockbox, host DMA, rotary encoder, stereo audio codec	Up to 48	8 GP, WD, RTC	1.225	1.8, 2.5, 3.3	93	12 mm × 12 mm, 0.5 mm, 289 CSP_BGA	0°C to +70°C		9.89	Production
ADSP-BF522C	400	800										1.40		158	12 mm × 12 mm, 0.5 mm, 289 CSP_BGA	0°C to +70°C		12.04	
ADSP-BF523C	533	1066										1.15		166	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		15.63	Production
ADSP-BF523C	600	1200										1.20		205	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		19.24	
ADSP-BF524C	300	600						USB 2.0 HS OTG, 2 UARTs, 2 SPORTs, SPI, TWI				1.225		93	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		11.29	Production
ADSP-BF524C	400	800										1.40		158	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		13.74	
ADSP-BF525C	533	1066										1.15		166	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		17.37	Production
ADSP-BF525C	600	1200										1.20		205	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		21.00	
ADSP-BF526C	300	600							Ethernet MAC, PPI/LCD, Lockbox, host DMA, rotary encoder, stereo audio codec			1.225		93	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		12.47	Production
ADSP-BF526C	400	800										1.40		158	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA	0°C to +70°C		15.53	
ADSP-BF527C	533	1066										1.15		166	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	0°C to +70°C		19.24	Production
ADSP-BF527C	600	1200										1.20		205	12 mm × 12 mm, 0.5 mm, 289-ball CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	0°C to +70°C		22.89	
ADSP-BF531	400	800	16k SRAM/cache + 16k SRAM	16k SRAM/cache (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM	12	UART, 2 SPORTs, SPI	PPI/LCD	16	3 GP, WD, RTC	1.20	1.8, 2.5, 3.3	150	12 mm × 12 mm, 0.8 mm, 160 CSP_BGA	−40°C to +85°C	−40°C to +105°C; −40°C to +85°C	5.99	Production
ADSP-BF531															19 mm × 19 mm, 1.0 mm, 169-ball PBGA	−40°C to +85°C	—		
ADSP-BF531															24 mm × 24 mm, 0.5 mm, 176-lead LQFP	0°C to +85°C	—		
ADSP-BF532	400	800	16k SRAM/cache + 32k SRAM	32k SRAM/cache (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM	12	UART, 2 SPORTs, SPI	PPI/LCD	16	3 GP, WD, RTC	1.20	1.8, 2.5, 3.3	150	12 mm × 12 mm, 0.8 mm, 160 CSP_BGA	−40°C to +85°C	−40°C to +105°C; −40°C to +85°C	9.33	Production
ADSP-BF532															19 mm × 19 mm, 1.0 mm, 169-ball PBGA	−40°C to +85°C	—		
ADSP-BF532															24 mm × 24 mm, 0.5 mm, 176-lead LQFP	0°C to +85°C	—		

Single Core

Part Number	Clock Speeds (MHz)	16-Bit Fixed-Point MMACS	On-Chip L1 Program (Bytes)	On-Chip L1 Data (Bytes)	Other Internal Memory (Bytes)	External Memory Type Supported	DMA (Channels)	Serial Ports	Other Ports/Features	Number of GPIOs	Timers	Core V_DDINT (Max Speed)	External (I/O)	Total Core Power Typ (mW)[3]	Package[4,5]	Temperature Range (Nonautomotive Grade)	Temperature Range Automotive Grade (W)[2]	Price @ 1k ($U.S.)[6]	Availability
ADSP-BF533	400	800	16k SRAM/cache + 64k SRAM	32k SRAM/cache + 32k SRAM (+ 4k scratchpad)	—	Async, SDRAM, mobile SDRAM	12	UART, 2 SPORTs, SPI	PPI/LCD	16	3 GP, WD, RTC	1.20	1.8, 2.5, 3.3	150	24 mm × 24 mm, 0.5 mm, 176-lead LQFP; 19 mm × 19 mm, 1.0 mm, 169-ball PBGA; 12 mm × 12 mm, 0.8 mm, 160-ball CSP_BGA		—	12.19	Production
	500	1000										1.20		228	19 mm × 19 mm, 1.0 mm, 169-ball PBGA; 12 mm × 12 mm, 0.8 mm, 160-ball CSP_BGA	−40°C to +85°C	−40°C to +105°C	15.33	
	533	1066										1.25		250	12 mm × 12 mm, 0.8 mm, 160-ball CSP_BGA	−40°C to +85°C	−40°C to +85°C	15.15	
	600	1200										1.30		319	12 mm × 12 mm, 0.8 mm, 160-ball CSP_BGA	0°C to +70°C	—	20.19	
ADSP-BF534	400	800		32k SRAM/cache + 32k SRAM (+ 4k scratchpad)	—				2 UARTs, 2 SPORTs, SPI, TWI, CAN	PPI/LCD	Up to 48	8 GP, WD, RTC	1.20	2.5, 3.3	150	17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +105°C	−40°C to +105°C	18.53	Production
															12 mm × 12 mm, 0.8 mm, 182-ball CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	−40°C to +85°C	12.40	
	500	1000										1.20		210	12 mm × 12 mm, 0.8 mm, 182-ball CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	—	15.39	
ADSP-BF536	300	600							Ethernet MAC, PPI/LCD			1.20		120	12 mm × 12 mm, 0.8 mm, 182-ball CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	—	10.07	
	400	800										1.20		150				13.11	
ADSP-BF537	500	1000										1.20		210	12 mm × 12 mm, 0.8 mm, 182 CSP_BGA; 17 mm × 17 mm, 0.8 mm, 208-ball CSP_BGA	−40°C to +85°C	—	17.15	
	533	1066										1.25		231		0°C to +70°C		19.09	
	600	1200										1.30		295				21.20	
ADSP-BF538	400	800	16k SRAM/cache + 48k SRAM		—	Async, SDRAM	28	3 UARTs, 4 SPORTs, 3 SPIs, 2 TWIs, CAN	PPI/LCD	Up to 54	3 GP, WD, RTC	1.20	2.5, 3.3	156	17 mm × 17 mm, 0.8 mm, 316-ball CSP_BGA	−40°C to +85°C	−40°C to +85°C	16.03	
	533	1066										1.25		225				16.28	
ADSP-BF538F	400	800			1M parallel flash							1.20	3.0, 3.3	156				20.26	
	533	1066										1.25		225				20.67	Production
ADSP-BF539	533	1066			—		34		PPI/LCD, MXVR			1.25	2.5, 3.3	225	17 mm × 17 mm, 0.8 mm, 316-ball CSP_BGA	—		Contact ADI	
ADSP-BF539F	533	1066			512k/1M parallel flash							1.25	3.0, 3.3	225		—		Contact ADI	
ADSP-BF542	400	800			—		28	USB 2.0 HS OTG, 3 UARTs, 3 SPORTs, 2 SPIs, TWI, CAN	ePPI/LCD, ATAPI, SDIO, keypad, rotary, pixel compositor, Lockbox	Up to 152	8 GP, WD, RTC	1.20	2.5, 3.3	239	17 mm × 17 mm, 0.8 mm, 400-ball CSP_BGA	—	—	15.66	
	533	1066										1.25	2.5, 3.3, 1.23 (mDDR)	376		−40°C to +85°C	−40°C to +85°C	17.40	Production
ADSP-BF544	600	1200						3 UARTs, 3 SPORTs, 2 SPIs, 2 TWIs, 2 CANs	2 ePPI/LCD, host dma keypad, rotary, pixel compositor, Lockbox		11 GP, WD, RTC	1.35	2.5, 3.3, 1.23	462		0°C to +70°C	—	19.14	
	400	800										1.20	2.5, 3.3	239		−40°C to +85°C	—	16.56	
	533	1066			64k L2 SRAM	Async, DDR1, NAND flash (mDDR option for 533 MHz grade only)						1.25	2.5, 3.3, 1.23 (mDDR)	376		−40°C to +85°C	−40°C to +85°C	18.40	
ADSP-BF547	533	1066						USB 2.0 HS OTG, 4 UARTs, 4 SPORTs, 4 SPIs, 2 TWIs	2 ePPI/LCD, ATAPI, SDIO, host dma, keypad, rotary, pixel compositor, Lockbox		11 GP, WD, RTC	1.25	2.5, 3.3, 1.23 (mDDR)	376	17 mm × 17 mm, 0.8 mm, 400-ball CSP_BGA	−40°C to +85°C	—	20.11	
	600	1200			128k L2 SRAM							1.35	2.5, 3.3	462		0°C to +70°C		22.12	
ADSP-BF548	533	1066						USB 2.0 HS OTG, 4 UARTs, 4 SPORTs, 3 SPIs, 2 TWIs, 2 CANs				1.25	2.5, 3.3, 1.23 (mDDR)	376	17 mm × 17 mm, 0.8 mm, 400-ball CSP_BGA	−40°C to +85°C	—	20.71	

Part Number	Performance		Memory				DMA (Channels)	Peripheral Options[1]				Voltage (V) Nominal[2]		Total Core Power Typ (mW)[3]	Packaging and Operating Temperature Range Options[4,5]			Price @ 1k ($U.S.)[6]	Availability
	Clock Speeds (MHz)	16-Bit Fixed-Point MMACS	On-Chip L1 Program (Bytes)	On-Chip L1 Data (Bytes)	Other Internal Memory (Bytes)	External Memory Type Supported		Serial Ports	Other Ports/Features	Number of GPIOs	Timers	Core V$_{DDINT}$ (Max Speed)	External (I/O)		Package[4,5]	Temperature Range (Nonautomotive Grade)	Temperature Range Automotive Grade (W)[2]		
Single Core																			
ADSP-BF535	200	400	16k SRAM/cache	32k SRAM/cache	256k L2 SRAM	Async, SDRAM	12	2 UARTs, 2 SPORTs, 2 SPIs, USB 1.1	PCI, PWM	16	3 GP, WD, RTC	1.20	3.3	247	19 mm × 19 mm, 1.0 mm, 260-ball PBGA	–40°C to +85°C, 0°C to +70°C	—	31.27	Production
	300	600										1.50		580				34.40	
	350	700										1.60		796				43.00	
Dual Core																			
ADSP-BF561	500	2000	16k SRAM/cache + 16k SRAM (per core)	32k SRAM/cache + 32k SRAM (per core)	128k L2 SRAM	Async, SDRAM	24	UART, 2 SPORTs, SPI	2 PPI/LCD	Up to 48	12 GP, 2 WD	1.25	2.5, 3.3	825	12 mm × 12 mm, 0.65 mm, 256-ball CSP_BGA	0°C to +70°C	—	20.40	Production
															17 mm × 17 mm, 1.0 mm, 256-ball CSP_BGA; 27 mm × 27 mm, 1.0 mm, 297-ball PBGA	–40°C to +85°C, 0°C to +70°C			
	533	2132										1.25		964	17 mm × 17 mm, 1.0 mm, 256-ball CSP_BGA; 27 mm × 27 mm, 1.0 mm, 297-ball PBGA	—	–40°C to +105°C	Contact ADI	
															12 mm × 12 mm, 0.65 mm, 256-ball CSP_BGA	0°C to +70°C		27.70	
	600	2400										1.35		1104	27 mm × 27 mm, 1.0 mm, 297-ball PBGA	–40°C to +85°C, 0°C to +70°C	—	29.13	
															12 mm × 12 mm, 0.65 mm, 256-ball CSP_BGA; 17 mm × 17 mm, 1.0 mm, 256-ball CSP_BGA	0°C to +70°C			

NOTES

[1] Due to pin muxing options, not all peripheral combinations may be available simultaneously. Please refer to data sheet and user manuals for full information.

[2] Automotive grade products may require different voltage conditions. Please refer to data sheet for full information.

[3] Core power (mW) stated for maximum core operating speed of the device at T$_J$ = 25°C, ASF = 1.0 (Using V$_{DDINT}$ nominal and I$_{DD,TYP}$ supply current for typical activity. Typical activity is the core executing an application comprised of 75% dual-MAC instructions and 25% dual-ALU instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled). Please refer to associated data sheet and EE notes for further details and complete power calculation information. Dynamic power management available via software programmable PLL, core voltage modifications, and a number of power-down modes. ADSP-BF522, ADSP-BF524, ADSP-BF526, ADSP-BF51x, and ADSP-BF50x products offer lowest deep-sleep power and less power variation over temperature.

[4] All DSP products available in RoHS compliant options. Please refer to data sheet for complete information.

[5] All packaging, operating temperature, and grade combinations may not be available. Please refer to data sheet for full information and contact ADI for options outside those listed.

[6] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate the lowest priced version of that particular speed device and will vary depending on package type and/or temperature range and grade.

[7] Pricing, power, and core voltage are subject to change. Please contact ADI for further information.

ADSP-BF592 Blackfin Processor
Low Cost with Optimized Peripheral Set for Industrial and General-Purpose Applications

The ADSP-BF592 is the low cost entry point into the Blackfin portfolio of processors. With core clock speeds of 200 MHz and 400 MHz and a peripheral set including two SPORTs, a PPI, two SPIs, four general-purpose counters and a factory-programmed instruction ROM block containing the VDK RTOS and C runtime libraries, the ADSP-BF592 is feature and cost optimized for compute intensive industrial, automotive, and general-purpose applications that do not require external memory or executable flash. The ADSP-BF592 is offered in a low cost 9 mm × 9 mm LFCSP package in commercial and industrial temperature grades as well as automotive qualified.

Features

- Blackfin processor core with 400 MHz (800 MMACS) performance and 68 kB L1 memory
- L1 instruction ROM block with VDK RTOS and C runtime libraries
- Low power dissipation of 51mW at 200 MHz
- 2 SPIs, 2 SPORTs, 2 UARTs, and 1 PPI
- 4 general-purpose counters, 3 with PWM support
- 9 peripheral DMA channels and 2 memory to memory DMA channels
- 9 mm × 9 mm LFCSP package
- Commercial, industrial, and automotive temperature grades

Markets and Applications

- Consumer audio
- Low cost imaging devices
- Smart meters
- Consumer handheld devices
- Medical equipment
- Automotive driver assistance systems

ADSP-BF592 Block Diagram
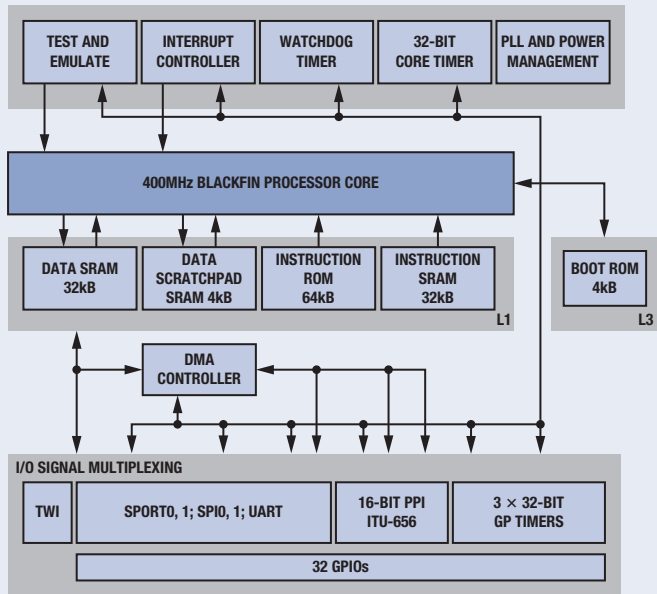
Part Number	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price @ 1k ($U.S.)[1]
ADSP-BF592BCPZ	400	800	68	−40°C to +85°C	SPI, PPI, SPORT, UART	64-lead LFCSP	4.33
ADSP-BF592KCPZ	400	800	68	0°C to +70°C			3.55
ADSP-BF592KCPZ-2	200	400	68	0°C to +70°C			1.99

NOTES
[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.
Z = RoHS compliant part.

ADSP-BF504/ADSP-BF504F/ADSP-BF506F Blackfin Processors
Low Power and Cost Optimized with Optional Integrated Executable Flash and 12-Bit ADC

The ADSP-BF50x family of processors brings a new level of system integration to the Blackfin portfolio by combining a high performance Blackfin processor with a 4 MB executable flash memory and a 12-bit, dual SAR ADC. Additionally, with a peripheral set including multiple serial interfaces, a parallel port interface, a CAN controller, two UARTs, eight general-purpose timers, and two 3-phase PWM interfaces, the ADSP-BF50x family is well suited for a variety of industrial and instrumentation applications. The 12-bit, dual SAR ADC is a hallmark feature of the ADSP-BF506F. This integrated signal conversion capability based on Analog Devices legendary analog signal processing technology meets the demanding requirements of a multitude of advanced power electronics applications, including motor control, universal power supply, and alternative energy inverters, as well as many other signal processing applications. An integrated ADC control module peripheral on the ADSP-BF50x family enables highly synchronized and precise control of the ADC's input sampling, eliminating the need for less precise software-based control or more expensive external logic-based control.

The ADSP-BF50x family of processors offers a highly optimized memory architecture that combines 68 kB of core L1 memory with 4 MB of synchronous burst flash memory that can be used for program execution, as well as data and boot code storage. This ample memory storage allows system designers to eliminate costly and power hungry external SDRAM chips and also serves to reduce the pin count, package size, and cost of the ADSP-BF50x processors vs. processors that provide external memory interfaces.

For low cost, low power, small memory footprint applications, the ADSP-BF50x family of processors offers best-in-class processor performance in its price range enabling advanced signal processing capabilities that previously weren't possible due to price constraints of competitive processors on the market. Addressing the need for integration of external mass storage devices, the removable storage interface of the ADSP-BF50x family of processors supports popular removable storage options such as MMC and SD, as well as providing an interface to wireless interfaces such as Bluetooth.

Features

- Blackfin processor core with up to 400 MHz (800 MMACS) performance
- 68 kB L1 SRAM and optional 4 MB synchronous, parallel burst flash memory
- Optional 12-bit, dual SAR ADC
- ADC control module for precise ADC sampling of inputs
- Two 3-phase PWM units
- Connectivity: SDIO, CE-ATA, eMMC, UARTs, SPORTs, SPI, PPI, CAN and TWI
- 8 general-purpose counters

- 12 peripheral DMA channels supporting one- and two-dimensional data transfers
- Multiple low power modes, including external voltage regulator interface with multiple GPIO wakeup.
- 120-lead, 0.4 mm pitch, 14 mm × 14 mm LQFP (ADSP-BF506F)
- 88-lead, 0.5 mm pitch, 12 mm × 12 mm LFCSP (ADSP-BF504 and ADSP-BF504F)
- Commercial and industrial temperature range

Applications

- Motor control
- Uninterruptible power supplies
- Programmable logic controllers
- Alternative energy inverters
- Biometric systems
- Medical devices
- Consumer audio
- Automotive
- Games/learning aids
- Industrial and instrumentation
- Portable test equipment
- PMPs
- Cameras
- Image scanners

ADSP-BF50x Block Diagram
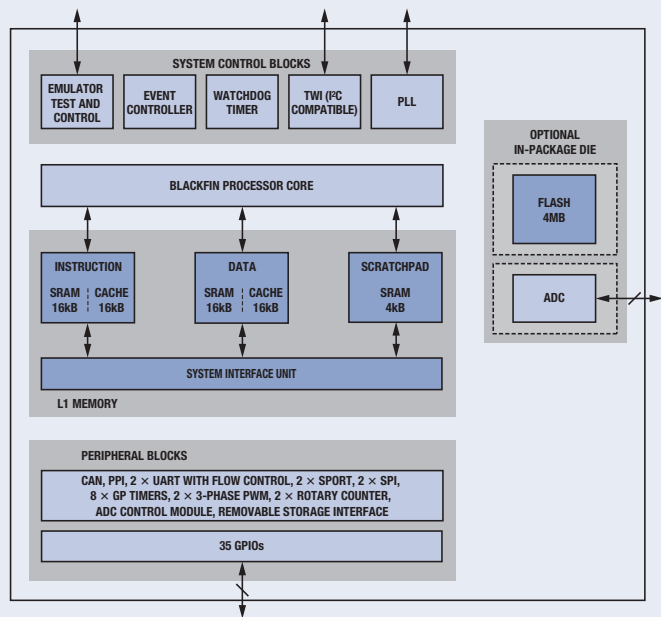
ADSP-BF504/ADSP-BF504F/ADSP-BF506F Blackfin Processors
Low Power and Cost Optimized with Optional Integrated Executable Flash and 12-Bit ADC

Part Number	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @1k ($U.S.)[1]
ADSP-BF504BCPZ-4	400	800	68	−40 to +85	2 SPIs, PPI, 2 SPORTs, 2 UARTs, CAN, 2 PWMs, ADC control module	88-lead LFCSP	
ADSP-BF504KCPZ-4	400	800	68	0 to 70		88-lead LFCSP	
ADSP-BF504BCPZ-3F	300	600	68	−40 to +85	2 SPIs, PPI, 2 SPORTs, 2 UARTs, CAN, 2 PWMs, ADC control module, 4 MB parallel flash	88-lead LFCSP	
ADSP-BF504KCPZ-3F	300	600	68	0 to 70		88-lead LFCSP	
ADSP-BF504BCPZ-4F	400	800	68	−40 to +85		88-lead LFCSP	5.18 to 13.78[2]
ADSP-BF504KCPZ-4F	400	800	68	0 to 70		88-lead LFCSP	
ADSP-BF506BSWZ-3F	300	600	68	−40 to +85	2 SPIs, PPI, 2 SPORTs, 2 UARTs, CAN, 2 PWMs, ADC control module, 4 MB parallel flash, 12-bit ADC	120-lead LQFP E-Pad	
ADSP-BF506KSWZ-3F	300	600	68	0 to 70		120-lead LQFP E-Pad	
ADSP-BF506BSWZ-4F	400	800	68	−40 to +85		120-lead LQFP E-Pad	
ADSP-BF506KSWZ-4F	400	800	68	0 to 70		120–lead LQFP E-Pad	

NOTES

[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

[2] Pricing is subject to change. Please contact ADI for further information.

Z = RoHS compliant part.

ADSP-BF512/ADSP-BF514/ADSP-BF516/ADSP-BF518 Blackfin Processors
Low Power with Advanced Embedded Connectivity

The Blackfin processor family is extended further into the industrial and instrumentation market by the introduction of the ADSP-BF51x family, which offers the availability of an on-chip eMAC that supports IEEE 1588 (version 2), a 3-phase PWM generation unit, and a quadrature encoder.

The high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of connected applications, including motor control, power line monitoring, biometrics, pro-audio, and femtocells.

The embedded eMAC of the ADSP-BF518F is fully compliant with the IEEE 1588 standard, version 2. With the time stamping mechanism being on the processor, users are free to chose any PHY they want to implement a 1588-based system. This, coupled with a 400 MHz CPU and a plethora of other peripherals, makes the ADSP-BF51x the most attractive choice for demanding network connected systems.

The VoIP challenge to the embedded system designer is to choose a processing solution that is cost-effective, easy to deploy, and scalable in performance across market spaces. A "sweet spot" embedded solution approach is to design with a platform that can implement a low channel count basic VoIP solution yet retain sufficient capacity for value added capabilities and services—such as video, music, imaging, and system control. Unlike traditional VoIP embedded solutions that utilize two processor cores to provide VoIP functionality, the ADSP-BF516 and ADSP-BF518 provide a convergent solution in a unified core architecture that allows voice and video signal processing concurrent with RISC MCU processing to handle network and user-interface demands. This unique ability to offer full VoIP functionality on a single convergent processor provides for a unified software development environment, faster system debugging and deployment, and lower overall system cost.

IP protection has become a necessary part of today's embedded computing applications. The ADSP-BF51x products provide a security scheme that balances flexibility and upgradeability with performance through the inclusion of a firmware-based solution including OTP (one-time programmable) memory to enable users to implement private keys for secure access to program code.

Features

- Blackfin processor core with up to 400 MHz (800 MMACS) performance
- 2 dual-channel, full-duplex synchronous serial ports supporting 8 stereo I²S channels
- 12 peripheral DMA channels supporting one- and two-dimensional data transfers
- Ethernet 10/100 MII interface with IEEE 1588 v2 support
- Connectivity: SDIO, CE-ATA, eMMC, UARTs, SPORTs, SPI and TWI
- Lockbox Secure Technology: hardware-enabled security for code and content protection
- Memory controller providing glueless connection to multiple banks of external SDRAM, SRAM, flash, or ROM
- 176-lead, 0.5 mm pitch, 24 mm × 24 mm LQFP
- 168-ball, 0.8 mm pitch, 12 mm × 12 mm CSP_BGA

Applications

- Biometric systems
- Consumer audio
- Games/learning aids
- Industrial and instrumentation
- Portable test equipment
- PMPs
- Wi-Fi devices
- Cameras
- Medical devices
- VoIP
- Industrial control
- Motor control
- Networked audio
- Femtocells

ADSP-BF51x Block Diagram
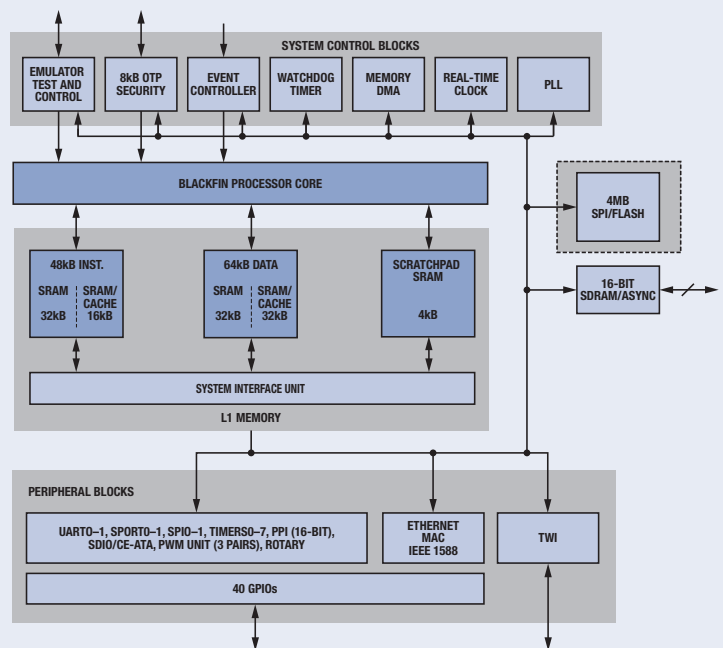
ADSP-BF512/ADSP-BF514/ADSP-BF516/ADSP-BF518 Blackfin Processors
Low Power with Advanced Embedded Connectivity

Part Number	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-BF512BBCZ-3	300	600	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs	168-ball CSP_BGA	6.26 to 10.31
ADSP-BF512BBCZ-4	400	800	116	−40 to +85		168-ball CSP_BGA	
ADSP-BF512BSWZ-3	300	600	116	−40 to +85		176-lead LQFP	
ADSP-BF512BSWZ-4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF512KBCZ-3	300	600	116	0 to 70		168-ball CSP_BGA	
ADSP-BF512KBCZ-4	400	800	116	0 to 70		168-ball CSP_BGA	
ADSP-BF512KSWZ-3	300	600	116	0 to 70		176-lead LQFP	
ADSP-BF512KSWZ-4	400	800	116	0 to 70		176-lead LQFP	
ADSP-BF512BBCZ-4F4	400	800	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, SPI flash	168-ball CSP_BGA	
ADSP-BF512BSWZ-4F4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF512KBCZ-4F4	400	800	116	0 to 70		168-ball CSP_BGA	
ADSP-BF512KSWZ-4F4	400	800	116	0 to 70		176-lead LQFP	
ADSP-BF514BBCZ-3	300	600	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, SDIO, CE-ATA, eMMC	168-ball CSP_BGA	7.77 to 10.88
ADSP-BF514BBCZ-4	400	800	116	−40 to +85		168-ball CSP_BGA	
ADSP-BF514BSWZ-3	300	600	116	−40 to +85		176-lead LQFP	
ADSP-BF514BSWZ-4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF514KBCZ-3	300	600	116	0 to 70		168-ball CSP_BGA	
ADSP-BF514KBCZ-4	400	800	116	0 to 70		168-ball CSP_BGA	
ADSP-BF514KSWZ-3	300	600	116	0 to 70		176-lead LQFP	
ADSP-BF514KSWZ-4	400	800	116	0 to 70		176-lead LQFP	
ADSP-BF514BBCZ-4F4	400	800	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, SDIO, CE-ATA, eMMC, SPI flash	168-ball CSP_BGA	
ADSP-BF514BSWZ-4F4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF514KBCZ-4F4	400	800	116	0 to 70		168-ball CSP_BGA	
ADSP-BF514KSWZ-4F4	400	800	116	0 to 70		176-lead LQFP	
ADSP-BF516BBCZ-3	300	600	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, 10/100 Ethernet, SDIO, CE-ATA, eMMC	168-ball CSP_BGA	8.92 to 12.03
ADSP-BF516BBCZ-4	400	800	116	−40 to +85		168-ball CSP_BGA	
ADSP-BF516BSWZ-3	300	600	116	−40 to +85		176-lead LQFP	
ADSP-BF516BSWZ-4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF516KBCZ-3	300	600	116	0 to 70		168-ball CSP_BGA	
ADSP-BF516KBCZ-4	400	800	116	0 to 70		168-ball CSP_BGA	
ADSP-BF516KSWZ-3	300	600	116	0 to 70		176-lead LQFP	
ADSP-BF516KSWZ-4	400	800	116	0 to 70		176-lead LQFP	
ADSP-BF516BBCZ-4F4	400	800	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, 10/100 Ethernet, SDIO, CE-ATA, eMMC, SPI flash	168-ball CSP_BGA	
ADSP-BF516BSWZ-4F4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF516KBCZ-4F4	400	800	116	0 to 70		168-ball CSP_BGA	
ADSP-BF516KSWZ-4F4	400	800	116	0 to 70		176-lead LQFP	
ADSP-BF518BBCZ-4	400	800	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, 10/100 Ethernet with 1588, SDIO, CE-ATA, eMMC, SPI flash	168-ball CSP_BGA	13.07 to 14.45
ADSP-BF518BSWZ-4	400	800	116	−40 to +85		176-lead LQFP	
ADSP-BF518BBCZ-4F4	400	800	116	−40 to +85	PPI, 2 SPIs, 2 SPORTs, TWI, 2 UARTs, 10/100 Ethernet with 1588, SDIO, CE-ATA, eMMC	168-ball CSP_BGA	
ADSP-BF518BSWZ-4F4	400	800	116	−40 to +85		176-lead LQFP	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Blackfin Processors

Low Power with Advanced Peripherals

The ADSP-BF52x Blackfin processor family combines high performance, power efficiency, and system integration to enable highly optimized designs without compromises. With built-in peripheral selectivity, the ADSP-BF52x family provides the greatest flexibility for today's most demanding convergent signal processing applications. With power consumption as low as 0.16 mW/MHz[1] and performance up to 600 MHz, applications can now add greater signal processing performance without sacrificing battery life. The ADSP-BF52x family supports peripheral flexibility and system scalability to enable developers to create products that fit their target needs.

The high performance 16-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of portable applications, including consumer, communications, and industrial/instrumentation.

IP protection has become a necessary part of today's embedded computing applications. The ADSP-BF52x family provides a security scheme that balances flexibility and upgradeability with performance through the inclusion of a firmware-based solution including OTP (one-time programmable) memory to enable users to implement private keys for secure access to program code.

[1] Referenced at 250 MHz operating speed for 300 MHz and 400 MHz ADSP-BF52x parts only.

Features

- Lockbox technology: hardware-enabled security for code and content
- Blackfin processor core with up to 600 MHz (1200 MMACS) performance
- 2 dual-channel, full-duplex synchronous serial ports supporting 8 stereo I²S channels
- 12 peripheral DMA channels supporting one- and two-dimensional data transfers
- NAND flash controller with 8-/16-bit interface for commands, addresses, and data
- Connectivity: HS USB OTG, host DMA port, UARTs, SPORTs, SPI, and TWI
- Ethernet 10/100 MII/RMII interface
- Memory controller providing glueless connection to multiple banks of external SDRAM, SRAM, flash, or ROM
- Wide range of operating voltages
- 289-ball, 12 mm × 12 mm, 0.5 mm pitch CSP_BGA (commercial temperature range 0°C to 70°C)
- 208-ball, 17 mm × 17 mm, 0.8 mm pitch CSP_BGA (industrial temperature range –45°C to +85°C)
- For space-constrained audio applications, the ADSP-BF52xC supports an embedded low power stereo codec

Applications

- VoIP
- Multimedia
- Multimedia accessories
- Home audio/video
- Instrumentation
- Imaging
- Industrial control
- PMP
- Mobile TV
- Coprocessor applications
- Networked audio
- Biometric systems
- Consumer audio
- Handheld and portable devices

ADSP-BF527 Block Diagram
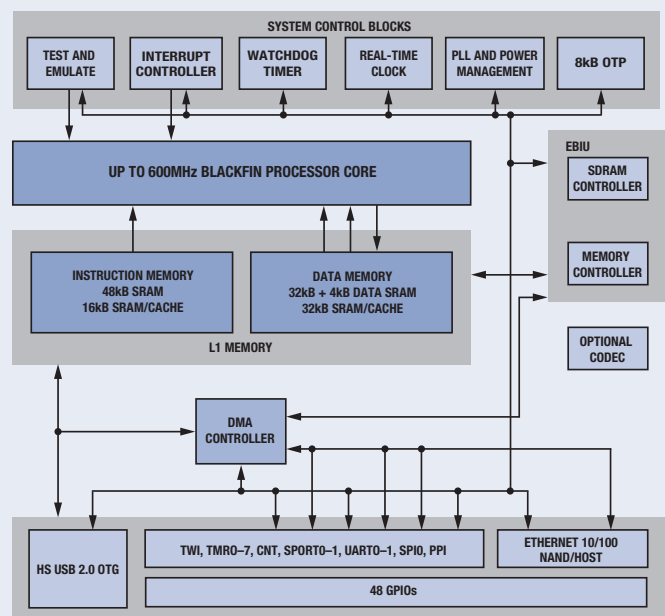
ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Blackfin Processors

Low Power with Advanced Peripherals

Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP–BF522BBCZ–3A	300	600	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF522BBCZ-4A	400	800	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF522KBCZ-3	300	600	132	0 to 70		289-ball CSP_BGA	8.18 to 12.04[4]
ADSP-BF522KBCZ-3C2[3]	300	600	132	0 to 70		289-ball CSP_BGA	
ADSP-BF522KBCZ-4	400	800	132	0 to 70	PPI, SPI, 2 SPORTs, NAND interface, TWI, host DMA, 2 UARTs, Lockbox	289-ball CSP_BGA	
ADSP-BF522KBCZ-4C2[3]	400	800	132	0 to 70		289-ball CSP_BGA	
ADSP-BF523BBCZ-5A	533	1066	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF523KBCZ-5	533	1066	132	0 to 70		289-ball CSP_BGA	
ADSP-BF523KBCZ-5C2[3]	533	1066	132	0 to 70		289-ball CSP_BGA	13.46 to 19.24
ADSP-BF523KBCZ-6	600	1200	132	0 to 70		289-ball CSP_BGA	
ADSP-BF523KBCZ-6A	600	1200	132	0 to 70		208-ball CSP_BGA	
ADSP-BF523KBCZ-6C2[3]	600	1200	132	0 to 70		289-ball CSP_BGA	
ADSP-BF524BBCZ-3A	300	600	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF524BBCZ-4A	400	800	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF524KBCZ-3	300	600	132	0 to 70		289-ball CSP_BGA	9.58 to 13.74[4]
ADSP-BF524KBCZ-3C2[3]	300	600	132	0 to 70		289-ball CSP_BGA	
ADSP-BF524KBCZ-4	400	800	132	0 to 70	PPI, SPI, 2 SPORTs, NAND interface, TWI, host DMA, 2 UARTs, Lockbox, HS USB OTG	289-ball CSP_BGA	
ADSP-BF524KBCZ-4C2[3]	400	800	132	0 to 70		289-ball CSP_BGA	
ADSP-BF525BBCZ-5A	533	1066	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF525KBCZ-5	533	1066	132	0 to 70		289-ball CSP_BGA	
ADSP-BF525KBCZ-5C2[3]	533	1066	132	0 to 70		289-ball CSP_BGA	15.17 to 21.00
ADSP-BF525KBCZ-6	600	1200	132	0 to 70		289-ball CSP_BGA	
ADSP-BF525KBCZ-6A	600	1200	132	0 to 70		208-ball CSP_BGA	
ADSP-BF525KBCZ-6C2[3]	600	1200	132	0 to 70		289-ball CSP_BGA	
ADSP-BF526BBCZ-3A	300	600	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF526BBCZ-4A	400	800	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF526KBCZ-3	300	600	132	0 to 70		289-ball CSP_BGA	10.76 to 15.53[4]
ADSP-BF526KBCZ-3C2[3]	300	600	132	0 to 70		289-ball CSP_BGA	
ADSP-BF526KBCZ-4	400	800	132	0 to 70	PPI, SPI, 2 SPORTs, 10/100 Ethernet, TWI, host DMA, NAND interface, 2 UARTs, Lockbox, HS USB OTG	289-ball CSP_BGA	
ADSP-BF526KBCZ-4C2[3]	400	800	132	0 to 70		289-ball CSP_BGA	
ADSP-BF527BBCZ-5A	533	1066	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF527KBCZ-5	533	1066	132	0 to 70		289-ball CSP_BGA	
ADSP-BF527KBCZ-5C2[3]	533	1066	132	0 to 70		289-ball CSP_BGA	16.99 to 22.89
ADSP-BF527KBCZ-6	600	1200	132	0 to 70		289-ball CSP_BGA	
ADSP-BF527KBCZ-6A	600	1200	132	0 to 70		208-ball CSP_BGA	
ADSP-BF527KBCZ-6C2[3]	600	1200	132	0 to 70		289–ball CSP_BGA	

NOTES

[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

[3] Stereo audio codec available.

[4] Pricing is subject to change. Please contact ADI for further information.

Z = RoHS compliant part.

ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548
Blackfin Processors
High Performance Convergent Multimedia Processors

The ADSP-BF54x family was specifically designed to meet the needs of convergent multimedia applications where system performance and cost are essential ingredients. The integration of multimedia, human interface, and connectivity peripherals combined with increased system bandwidth and on-chip memory provides customers a platform to design the most demanding applications.

IP protection has become a necessary part of today's embedded applications. The ADSP-BF54x provides a security scheme that balances flexibility and upgradeability with performance through the inclusion of a firmware-based solution including OTP memory to enable users to implement private keys for secure access to program code.

The ADSP-BF54x provides peripheral flexibility to complement its high performance processing. These rich system-level peripherals are well-suited for industrial multimedia and automotive infotainment applications where multiple standards are prevalent and system performance is required.

Features

- Powerful and flexible cache architecture suitable for soft real-time control tasks and industry-standard operating systems, plus hard real-time signal processing tasks
- Blackfin processor core with up to 600 MHz (1200 MMACS) performance
- Lockbox Secure Technology
- Two independent DMA controllers
- Human interface: 18-/24-bit LCD controller, 32-bit up/down counter/thumbwheel interface, 8 × 8 keypad interface
- Connectivity: high speed USB on-the-go (OTG) controller, host DMA, UARTs, SPORTs, SPI, TWI, and CAN (not available on ADSP-BF547)
- Expansion: SD/SDIO and ATAPI controllers
- Multimedia: 18-/24-bit LCD controller, multiple enhanced parallel peripheral interfaces (EPPI), pixel compositor hardware accelerator
- Asynchronous memory interface for SRAM, EEPROM, NAND/NOR flash connectivity
- Synchronous memory interface for DDR or Mobile DDR connectivity
- Core voltage: 0.9 V to 1.43 V

Applications

- Digital radio
- Audio jukebox
- Navigation
- Driver assistance
- Rear seat audio and video
- Advanced vehicle infotainment
- Mobile communications
- Security and access control systems
- Industrial control and factory automation
- Automotive driver assistance/safety
- Telecommunications radio and switches
- Security and access control systems
- Factory/building automation
- Automotive multimedia device interconnect
- PC peripherals
- POS barcode scanners

ADSP-BF54x Block Diagram
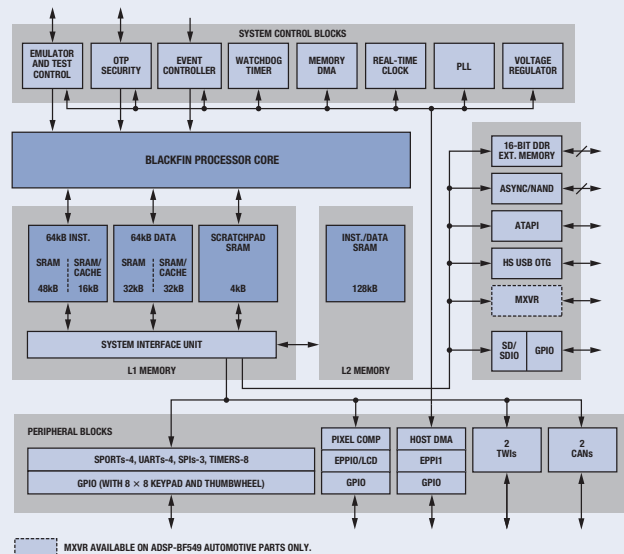
MXVR AVAILABLE ON ADSP-BF549 AUTOMOTIVE PARTS ONLY.

NOTE
PLEASE REFER TO INDIVIDUAL DATA SHEETS FOR SPECIFIC BLOCK DIAGRAMS.

ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548
Blackfin Processors
High Performance Convergent Multimedia Processors

Part Number[1,2]	Max (MHz)	Max (MMACS)	L1/L2 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[3]
ADSP-BF542BBCZ-4A	400	800	132/—	−40 to +85	CAN, HS USB OTG, 3 EPPIs, pixel comp, ATAPI-6, Lockbox	400-ball CSP_BGA	15.66 to 19.14
ADSP-BF542BBCZ-5A	533	1066	132/—	−40 to +85		400-ball CSP_BGA	
ADSP-BF542MBBCZ-5M	533	1066	132/—	−40 to +85		400-ball CSP_BGA	
ADSP-BF542KBCZ-6A	600	1200	132/—	0 to 70		400-ball CSP_BGA	
ADSP-BF544BBCZ-4A	400	800	132/64	−40 to +85	CAN, Host DMA, 3 EPPIs, pixel comp, Lockbox	400-ball CSP_BGA	16.56 to 18.40
ADSP-BF544BBCZ-5A	533	1066	132/64	−40 to +85		400-ball CSP_BGA	
ADSP-BF544MBBCZ-5M	533	1066	132/64	−40 to +85		400-ball CSP_BGA	
ADSP-BF547BBCZ-5A	533	1066	132/128	−40 to +85	HS USB OTC, 3 EPPIs, pixel comp, ATAPI-6, Lockbox	400-ball CSP_BGA	20.11 to 22.12
ADSP-BF547MBBCZ-5M	533	1066	132/128	−40 to +85		400-ball CSP_BGA	
ADSP-BF547KBCZ-6A	600	1200	132/128	0 to 70		400-ball CSP_BGA	
ADSP-BF548BBCZ-5A	533	1066	132/128	−40 to +85	HS USB OTG, 3 EPPIs, pixel comp, ATAPI-6, Lockbox, CAN	400-ball CSP_BGA	20.71
ADSP-BF548MBBCZ-5M	533	1066	132/128	−40 to +85		400-ball CSP_BGA	

NOTES
[1] Certain models available in automotive grade.

[2] Products without an M support standard DDR memory only.

[3] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

M = support for 1.8 V mobile DDR memory.

Z = RoHS compliant part.

ADSP-BF538/ADSP-BF538F Blackfin Processors
Embedded and Integrated Development

The Blackfin processor family has been expanded to address the ever increasing need for more connection possibilities with two new family members. This connectivity is coupled with the high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality. System designers can take advantage of the combined control and signal processing capabilities of the processor core across a wide range of end applications through code compatibility of these new family members with existing Blackfin offerings.

The ADSP-BF538 and ADSP-BF538F are functional extensions of the popular ADSP-BF533 processor (found on Page 42), and they are ideally suited for applications with multiple device connections. The ADSP-BF538 offers equivalent embedded memory and is well-suited for applications such as video security/surveillance and industrial-environment-based distributed control/factory automation applications. The ADSP-BF538F is equivalent in functionality to the ADSP-BF538 processor with the addition of on-board flash memory. Both devices are ideally suited for a broad range of industrial, instrumentation, and medical appliance applications—allowing for broad connection possibilities coupled with a mix of control and signal processing needs based in the end product.

ADSP-BF538/ADSP-BF538F Block Diagram
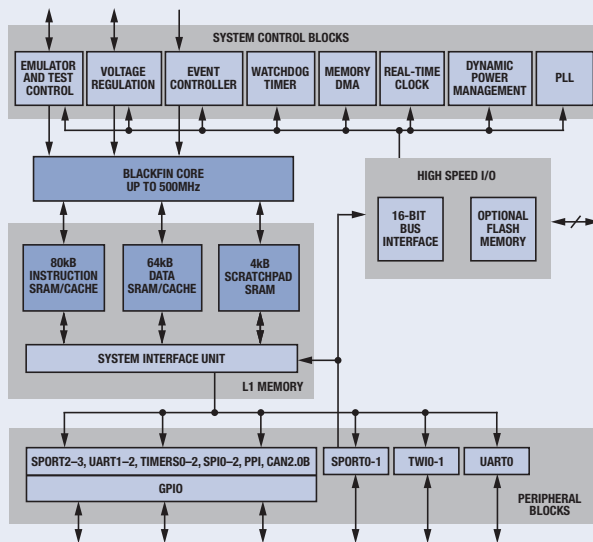
Features

- Powerful and flexible cache architecture suitable for soft real-time control tasks and industry-standard operating systems, plus hard real-time signal processing tasks
- Addition of on-board flash memory for code storage of complex system application that run on a powerful 400 MHz or 533 MHz processor
- Application-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications
- Enhanced dynamic power management with on-chip voltage regulation
- 10-stage RISC MCU/DSP pipeline with mixed 16-/32-bit ISA for optimal code density
- Full SIMD architecture, including instructions for accelerated video and image processing
- Memory management unit (MMU) supporting full memory protection for an isolated and secure environment
- More SPORT, UART, SPI, and TWI peripherals over the popular ADSP-BF533 processor
- Controller area network (CAN) 2.0B interface
- Enhanced DMA controller for high bandwidth throughput accommodating multiple peripherals
- 148 kB on-chip full-speed SRAM
- Glueless SDRAM, SRAM, and flash controllers
- 1 MB of flash memory on ADSP-BF538F devices
- Glueless video capture/display port
- 316-ball, lead-free CSP_BGA package
- Core voltage: 0.8 V to 1.375 V
- Industrial temperature range
- Multiple pin- and code-compatible derivatives

Applications

- Video security/surveillance
- Industrial
- Instrumentation
- Medical appliances

Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Flash Memory (Bytes)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF538BBCZ-4A	400	800	148	—	−40 to +85		316-ball CSP_BGA	
ADSP-BF538BBCZ-4F8	400	800	148	1M	−40 to +85	CAN 2.0B, 54 GPIOs, 4 SPORTs, 3 UARTs, 3 SPIs, 2 TWIs, PPI, 8 MB flash	316-ball CSP_BGA	16.03 to 20.67
ADSP-BF538BBCZ-5A	533	1066	148	—	−40 to +85		316-ball CSP_BGA	
ADSP-BF538BBCZ-5F8	533	1066	148	1M	−40 to +85		316-ball CSP_BGA	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-BF536/ADSP-BF537 Blackfin Processors
Embedded Network Connectivity

The Blackfin processor family addresses the ever increasing need for pervasive embedded network connectivity with the ADSP-BF536/ADSP-BF537. This connectivity is powerful when utilized in conjunction with the high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality. System designers can take advantage of the combined control and signal processing capabilities of the processor core across a wide range of end applications through the scalability of the pin and code compatibility of these new family members. The ADSP-BF536 and ADSP-BF537 are a functional extension of the popular ADSP-BF531, ADSP-BF532, and ADSP-BF533 processors (found on Page 40 to Page 42), and they are ideally suited for a variety of networked applications.

Designed for Endpoint Connectivity

The Blackfin processor core is ideally suited for handling both control-oriented networking tasks and user interface mechanisms while also offering full signal processing capabilities for analyzing almost any condition. To complement the performance, the Blackfin processor's memory system offers a powerful and flexible cache architecture that can dynamically balance between the hard real-time tasks desired in SRAM, the soft real-time control tasks, and an operating system (OS) requiring cache functionality. DPM lowers power consumption for extending battery life or for minimizing power dissipation in enclosed applications.

Designed for Bandwidth

The ADSP-BF536/ADSP-BF537 processors integrate a fully compliant IEEE 802.3-2002 standard 10/100 Ethernet MAC that has been enhanced with advanced features to allow for higher network bandwidth capabilities. In addition, the DMA subsystem has been enhanced with greater traffic management abilities to allow for higher data throughput with minimal processor core intervention. The DMA subsystem also includes dual external handshake DMA request lines that, when used in conjunction with the external bus interface unit (EBIU), can be used when a high speed interface is required for external FIFOs and high bandwidth communication peripherals, such as USB 2.0 devices. The

ADSP-BF536/ADSP-BF537 processors also embed a controller area network (CAN) module and are capable of data rates of up to 1 Mbps.

Features

- Up to 600 MHz operation
- Embedded IEEE 802.3 2002 compliant 10/100 Ethernet MAC and buffered oscillator output to a separate PHY
- Controller area network (CAN) 2.0B interface
- I²C®-compatible 2-wire interface
- Enhanced DMA controller, including two external handshake DMA request lines
- Up to 132 kB on-chip, full-speed SRAM
- Glueless SDRAM, SRAM, and flash controllers
- Glueless video capture/display port
- 182-ball and 208-ball CSP_BGA packages
- Lead-free and lead-bearing package options
- Industrial temperature ranges
- Core voltage: 0.8 V to 1.4 V

Applications

- Video security
- Video surveillance
- Industrial distributed control
- Industrial factory automation
- Remote monitoring devices
- Point-of-sale terminals
- VoIP
- Biometrics/security
- Instrumentation
- Medical appliances
- Consumer appliances

ADSP-BF536/ADSP-BF537 Blackfin Processors
Embedded Network Connectivity

ADSP-BF536/ADSP-BF537 Block Diagram
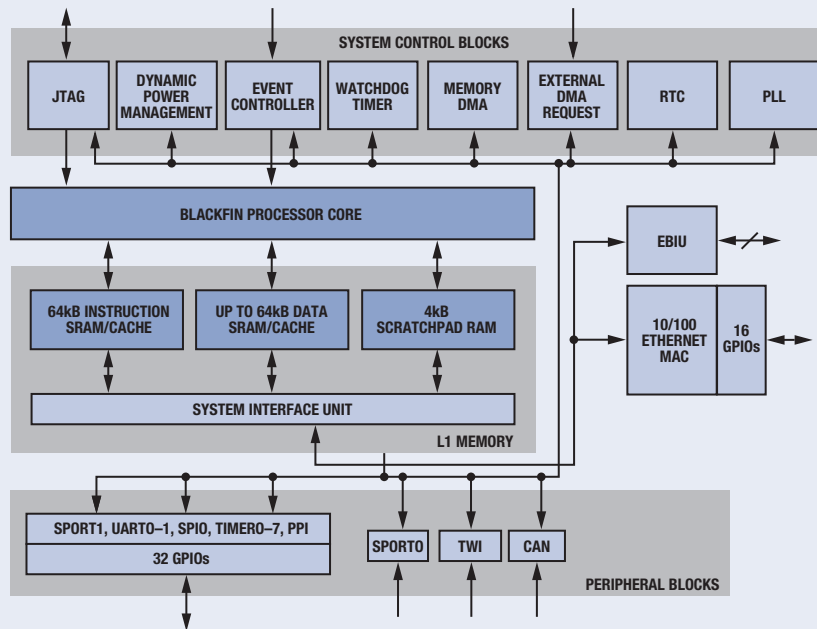
Part Number	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-BF536BBC-3A	300	600	100	−40 to +85		182-ball CSP_BGA	
ADSP-BF536BBCZ-3A	300	600	100	−40 to +85		182-ball CSP_BGA	
ADSP-BF536BBCZ-3B	300	600	100	−40 to +85		208-ball CSP_BGA	
ADSP-BF536BBC-4A	400	800	100	−40 to +85		182-ball CSP_BGA	10.07 to 15.14
ADSP-BF536BBCZ-4A	400	800	100	−40 to +85	10/100 Ethernet, CAN, PPI, TWI, 8 timers, 48 GPIOs, 2 SPORTs/ 2 UARTs, SPI	182-ball CSP_BGA	
ADSP-BF536BBCZ-4B	400	800	100	−40 to +85		208-ball CSP_BGA	
ADSP-BF537BBC-5A	500	1000	132	−40 to +85		182-ball CSP_BGA	
ADSP-BF537BBCZ-5A	500	1000	132	−40 to +85		182-ball CSP_BGA	
ADSP-BF537BBCZ-5B	500	1000	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF537BBCZ-5AV	533	1066	132	−40 to +85		182-ball CSP_BGA	17.15 to 21.20
ADSP-BF537BBCZ-5BV	533	1066	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF537KBCZ-6AV	600	1200	132	0 to 70		182-ball CSP_BGA	
ADSP-BF537KBCZ-6BV	600	1200	132	0 to 70		208-ball CSP_BGA	

NOTES
[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-BF534 Blackfin Processor
CAN Connectivity for Automotive and Industrial Applications

The ADSP-BF534 is a functional extension of the popular ADSP-BF531, ADSP-BF532, and ADSP-BF533 processors (found on Page 40 to Page 42) and is ideally suited for a variety of CAN networked applications. The ADSP-BF534 offers a high performance series for embedded applications such as automotive safety, automotive body control, automotive driver assistance, automotive entertainment, and industrial factory automation. This processor is ideally suited for a broad range of industrial, instrumentation, medical applications, and fleet monitoring that allows for scalability and CAN network connectivity utilizing a mix of control plus signal processing in the end product.

Designed for Endpoint Connectivity

Embedded CAN networked applications require ever increasing intelligence and analytical capabilities for endpoint decision making. The Blackfin processor core is ideally suited for handling both control-oriented networking tasks and user interface mechanisms while also offering full signal processing capabilities for analyzing almost any condition. To complement the performance, the Blackfin processor's memory system offers a powerful and flexible cache architecture that can dynamically balance the hard real-time tasks desired in SRAM, the soft real-time control tasks, and an operating system (OS) requiring cache functionality. Dynamic power management (DPM) lowers power consumption for extending battery life or for minimizing power dissipation in enclosed applications. DPM allows for independent dynamic scaling of either voltage or frequency in a self-contained system with the integration of both a voltage regulator and PLL that are software programmable.

Designed for Bandwidth

The ADSP-BF534 integrates a fully compliant CAN 2.0B module capable of data rates of up to 1 Mbps. This module supports up to 32 mailboxes with individual acceptance masks and data filtering. In addition, the DMA subsystem has been enhanced with greater traffic management abilities to allow for higher data throughput with minimal processor core intervention. The DMA subsystem also includes dual external handshake DMA request lines that, when used in conjunction with the external bus interface unit (EBIU), can be used when a high speed interface is required for external FIFOs and high bandwidth communication peripherals, such as USB 2.0 devices.

Features

- Up to 500 MHz operation
- Controller area network (CAN) 2.0B interface
- Enhanced DMA controller, including two external handshake DMA request lines
- 132 kB on-chip, full-speed SRAM
- Glueless SDRAM, SRAM, and flash controllers
- Glueless video capture/display port
- 8 timers supporting PWM and pulse width/event count modes
- 48 general-purpose I/Os, 8 with high source/high sink capabilities
- 182-ball and 208-ball sparse CSP_BGA packages
- Lead-free and lead-bearing package options
- Industrial and extended industrial temperature ranges
- Core voltage: 0.8 V to 1.2 V

Applications

- Automotive safety
- Automotive body control
- Automotive driver assistance
- Automotive entertainment
- Industrial factory automation
- Instrumentation
- Medical appliances
- Consumer appliances

ADSP-BF534 Block Diagram
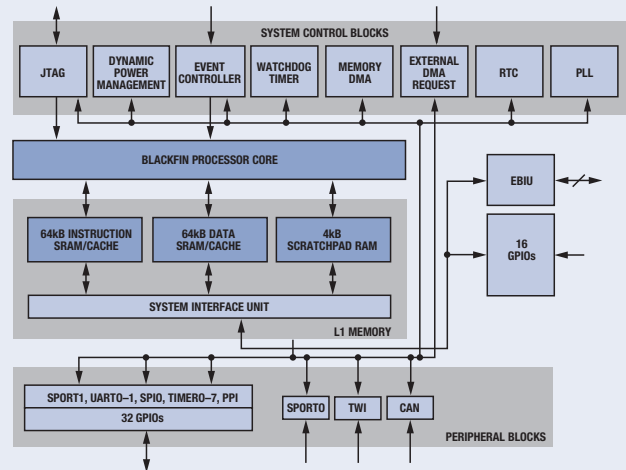
Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF534BBC-4A	400	800	132	−40 to +85		182-ball CSP_BGA	
ADSP-BF534BBCZ-4A	400	800	132	−40 to +85		182-ball CSP_BGA	
ADSP-BF534BBCZ-4B	400	800	132	−40 to +85	CAN, PPI/SPI, TWI, 8 timers, 48 GPIOs, 2 SPORTs/UARTs	208-ball CSP_BGA	12.40 to 18.53
ADSP-BF534BBC-5A	500	1000	132	−40 to +85		182-ball CSP_BGA	
ADSP-BF534BBCZ-5A	500	1000	132	−40 to +85		182-ball CSP_BGA	
ADSP-BF534BBCZ-5B	500	1000	132	−40 to +85		208-ball CSP_BGA	
ADSP-BF534YBCZ-4B	400	800	132	0 to 70		208-ball CSP_BGA	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-BF561 Blackfin Processor
Symmetric Multiprocessing

The Blackfin processor family expands the performance envelope with the introduction of the ADSP-BF561 configured as a symmetric multiprocessing arrangement of two Blackfin processor cores.

The ADSP-BF561 offers twice the signal processing performance of the ADSP-BF533 (found on Page 42), with more than twice the on-chip memory and significantly increased data bandwidth capability.

The ADSP-BF561 retains full code compatibility with the ADSP-BF533 and still maintains very low power consumption by using the dynamic power management capabilities of the Blackfin architecture.

The ADSP-BF561 integrates two Blackfin processor cores, each capable of operating at up to 600 MHz, and 2.6 Mb of on-chip SRAM memory. The on-chip memory is portioned between individual, high speed L1 memory for each core and a large 128 kB bank of shared L2 memory. Extremely high data bandwidth is provided by the 32-bit external port and dual 16-channel DMA controllers.

On-chip peripherals include dual parallel peripheral interfaces (PPIs), each with support for ITU-R 656 video formatting and high speed serial ports supporting I²S formats. The product is optimized for a variety of consumer multimedia and other processing intensive applications.

Features

- Dual Blackfin cores with each core capable of 600 MHz/1200 MMACS (2400 MMACS total)
- Large on-chip memory of 328 kB—arranged as individual L1 memory systems for each core, plus a shared L2 memory space
- High data throughput tailored for the needs of imaging and consumer multimedia applications
- Application-tuned peripherals provide glueless connectivity to a variety of audio/video converters and general-purpose ADCs/DACs
- Core voltage: 0.8 V to 1.4185 V

Applications

- Digital still cameras
- Digital video cameras
- Portable media players
- Digital video recorders
- Set-top boxes
- Consumer multimedia
- Automotive vision systems
- Broadband wireless systems
- Instrumentation
- Security and surveillance

ADSP-BF561 Block Diagram
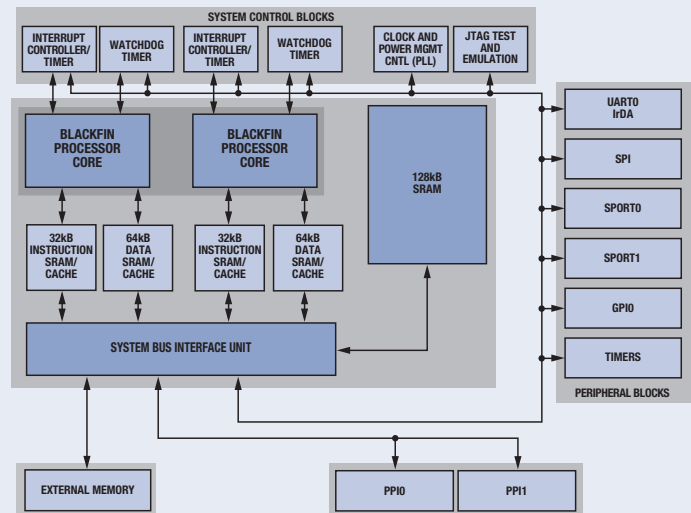
Part Number[1]	Max (MHz)	Max (MMACS)	L1/L2 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF561SBB500	500	2000	100[3]/128	−40 to +85		297-ball PBGA	
ADSP-BF561SBBZ500	500	2000	100[3]/128	−40 to +85		297-ball PBGA	
ADSP-BF561SBBCZ-5A	500	2000	100[3]/128	−40 to +85		256-ball CSP_BGA	
ADSP-BF561SKB500	500	2000	100[3]/128	0 to 70		297-ball PBGA	
ADSP-BF561SKBZ500	500	2000	100[3]/128	0 to 70		297-ball PBGA	
ADSP-BF561SKBCZ500	500	2000	100[3]/128	0 to 70	2 PPIs, UART, 12 timers, 2 SPORTs	256-ball CSP_BGA	20.40 to 37.53
ADSP-BF561SKBCZ-5A	500	2000	100[3]/128	0 to 70		256-ball CSP_BGA	
ADSP-BF561SKBCZ-5V	533	2000	100[3]/128	0 to 70		256-ball CSP_BGA	
ADSP-BF561SBB600	600	2400	100[3]/128	−40 to +85		297-ball PBGA	
ADSP-BF561SBBZ600	600	2400	100[3]/128	−40 to +85		297-ball PBGA	
ADSP-BF561SKB600	600	2400	100[3]/128	0 to 70		297-ball PBGA	
ADSP-BF561SKBZ600	600	2400	100[3]/128	0 to 70		297-ball PBGA	
ADSP-BF561SKBCZ-6A	600	2400	100[3]/128	0 to 70		256-ball CSP_BGA	
ADSP-BF561SKBCZ-6V	600	2400	100[3]/128	0 to 70		256-ball CSP_BGA	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

[3] Per core.

Z = RoHS compliant part.

ADSP-BF531/ADSP-BF532 Blackfin Processors
Low Power General-Purpose Applications

The ADSP-BF531 and ADSP-BF532 provide a low cost, power-efficient processor choice for today's most demanding convergent signal processing applications. With power consumption as low as 0.23 mW/MHz and performance of 400 MHz, applications can now add greater signal processing performance without sacrificing battery life.

The high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of applications, including consumer, communications, automotive, and industrial/instrumentation.

Designed for Performance and Power Efficiency

Both the ADSP-BF531 and the ADSP-BF532 offer 400 MHz performance and up to 800 MMACS. This processor core is supported by an advanced DMA controller supporting one- and two-dimensional DMA transfers between on-chip memory, off-chip memory, and system peripherals. The combination of the processor core speed and the DMA controller allows for efficient processing of audio, voice, video, and image data.

Blackfin processors also offer enhanced power management capabilities by integrating on-chip core voltage regulation circuitry. This on-chip voltage regulator allows for the core and system clocks to be dynamically modified via a digital divider circuit, providing systems designers an additional tool for optimization of power and performance in their end products.

Designed for Flexibility

With multiple package and memory options, many pin-for-pin-compatible, designers can choose the price point and cost point to meet their system requirements. Combined with a number of standard peripherals, including multifunction serial ports supporting I²S audio capability, UART, SPI-compatible port, three multifunction timers, and a programmable parallel port interface (PPI) with ITU-656 video support, the ADSP-BF531/ADSP-BF532 can address a wide variety of existing and emerging applications.

Designed for Low Cost

Both the ADSP-BF531 and the ADSP-BF532 were designed for cost-sensitive applications. By efficiently processing both control and signal processing code on a single processor, the Blackfin architecture eliminates the additional cost of having a separate digital signal processor in the system. Each product offers LQFP package options to simplify board design and peripherals like an on-chip real-time clock and voltage regulation to further reduce systems costs. The Blackfin processor's combination of performance, flexibility, and low cost is ideally suited for the most demanding convergent processing applications.

This processor family, combined with ADI's investment in future Blackfin products, provides a robust platform for tomorrow's most challenging convergent applications.

Features

- Performance to 400 MHz/800 MMACS enables multichannel audio plus CIF video processing in multimedia applications
- Enhanced dynamic power management with on-chip core voltage regulation allows operation to 0.8 V, extending battery life in portable applications
- Application-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications
- Multiple low cost, pin- and code-compatible derivatives enable software differentiation in cost-sensitive consumer applications
- Pin compatible with the ADSP-BF533 (found on Page 42)
- Core voltage: 0.8 V to 1.2 V

Applications

- Biometric systems
- Consumer audio
- Email terminals
- Embedded modems
- Games/learning aids
- Information appliances
- Industrial control
- Portable test equipment
- Web tablets/terminals
- Automotive telematics
- Consumer multimedia
- Digital and satellite radio
- Point-of-sale terminals
- Medical instrumentation
- Professional audio
- Telephony and communications
- Video conferencing
- VoIP terminals

ADSP-BF531/ADSP-BF532 Blackfin Processors

Low Power General-Purpose Applications

ADSP-BF531/ADSP-BF532 Block Diagram
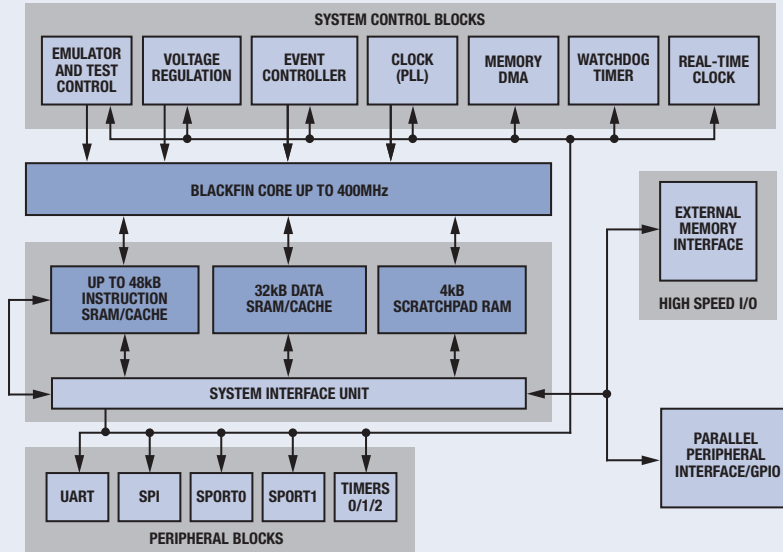
Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF531SBBC400	400	800	52	−40 to +85		160-ball CSP_BGA	
ADSP-BF531SBBCZ400	400	800	52	−40 to +85		160-ball CSP_BGA	
ADSP-BF531SBSTZ400	400	800	52	−40 to +85		176-lead LQFP	5.99 to 12.81
ADSP-BF531SBB400	400	800	52	−40 to +85		169-ball PBGA	
ADSP-BF531SBBZ400	400	800	52	−40 to +85	PPI, UART, SPI, 2 SPORTs, 3 timers, 16 GPIOs	169-ball PBGA	
ADSP-BF532SBBC400	400	800	84	−40 to +85		160-ball CSP_BGA	
ADSP-BF532SBBCZ400	400	800	84	−40 to +85		160-ball CSP_BGA	
ADSP-BF532SBSTZ400	400	800	84	−40 to +85		176-lead LQFP	9.33 to 17.31
ADSP-BF532SBB400	400	800	84	−40 to +85		169-ball PBGA	
ADSP-BF532SBBZ400	400	800	84	−40 to +85		169-ball PBGA	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-BF533 Blackfin Processor
High Performance General-Purpose Applications

The ADSP-BF533 provides a high performance, power-efficient processor choice for today's most demanding convergent signal processing applications. With performance up to 600 MHz (1200 MMACS), applications can now add greater signal processing performance without significantly increasing their system cost. The high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of applications, including consumer, communications, automotive, and industrial/instrumentation.

Designed for Performance

The ADSP-BF533 combines the high performance Blackfin core with large on-chip Level 1 cacheable instruction and data memories. This combination allows the ADSP-BF533 to achieve very high system performance for applications such as video or multimedia. This processor core is supported by an advanced DMA controller aiding one- and two-dimensional DMA transfers between on-chip memory, off-chip memory, and system peripherals. Blackfin processors also offer enhanced power management capabilities by integrating on-chip core voltage regulation circuitry. The on-chip voltage regulator and programmable PLL allow the core and system clocks to be dynamically modified via a digital divider circuit, providing systems designers an additional tool for optimization of power and performance in their end products.

Designed for Flexibility

With multiple package and memory options, designers can choose the price point and cost point to meet their system requirements. Combined with a number of standard peripherals, including multifunction serial ports supporting I²S audio capability, UART, SPI-compatible port, three multifunction timers, and a programmable parallel port interface (PPI) with ITU-656 video support, the ADSP-BF533 can address a wide variety of existing and emerging applications. Also, the ADSP-BF533 is code-compatible with all of the Blackfin family of processors, providing more choices and offering greater leverage across developments. The Blackfin processor's combination of performance and flexibility is ideally suited for the most demanding convergent processing applications. This processor family, combined with Analog Devices' investment in future Blackfin

products, provides a robust platform for tomorrow's most challenging convergent applications.
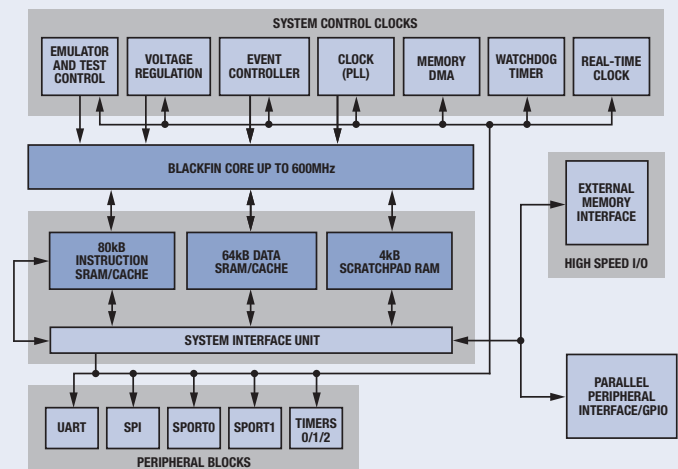
Features

- Up to 600 MHz performance
- 1200 MMACS
- Application-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications
- Large on-chip SRAM for maximum system performance
- Pin-compatible with the ADSP-BF531/ADSP-BF532 for scalable solutions
- Core voltage: 0.8 V to 1.45 V

Applications

- Multimedia
- Home audio/video
- Embedded modems
- Instrumentation
- Imaging
- Industrial control
- Voice communication

ADSP-BF533 Block Diagram

Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF533SBB500	500	1000	148	−40 to +85		169-ball PBGA	
ADSP-BF533SBBC400	400	800	148	−40 to +85		160-ball CSP_BGA	
ADSP-BF533SBBC500	500	1000	148	−40 to +85		160-ball CSP_BGA	
ADSP-BF533SBBC-5V	533	1066	148	−40 to +85		160-ball CSP_BGA	
ADSP-BF533SBBCZ400	400	800	148	−40 to +85		160-ball CSP_BGA	
ADSP-BF533SBBCZ500	500	1000	148	−40 to +85	PPI, UART, SPI,	160-ball CSP_BGA	
ADSP-BF533SBBCZ-5V	533	1066	148	−40 to +85	2 SPORTs,	160-ball CSP_BGA	12.19 to 23.32
ADSP-BF533SBBZ400	400	800	148	−40 to +85	3 timers, 16 GPIOs	169-ball PBGA	
ADSP-BF533SBBZ500	500	1000	148	−40 to +85		169-ball PBGA	
ADSP-BF533SBST400	400	800	148	−40 to +85		176-lead LQFP	
ADSP-BF533SBSTZ400	400	800	148	−40 to +85		176-lead LQFP	
ADSP-BF533SKBC-6V	600	1200	148	0 to 70		160-ball CSP_BGA	
ADSP-BF533SKBCZ-6V	600	1200	148	0 to 70		160-ball CSP_BGA	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-BF535 Blackfin Processor
High Performance Processor for Internet Appliances

The ADSP-BF535 high performance processor features dual MACs, high clock rates, and dynamic power management, allowing for optimization of system performance and power consumption. Additionally, through the advantages of a clean, orthogonal RISC instruction set, the ADSP-BF535 is optimized for programming in high level languages (HLL) like C/C++, resulting in extremely dense code.

At the heart of the Blackfin processor is ADI's most advanced 16-bit digital signal processing core architecture. This new core has three primary objectives—performance, power management, and ease of use.

High Performance

Blackfin processors employ a dual-MAC processor that also includes efficient RISC MCU system control functionality and multimedia processing capabilities. All are combined into one simple, optimized instruction set architecture.

Dynamic Power Management

Blackfin processor's dynamic power management offers a flexible, software controlled environment that delivers the required amount of performance to the processor via independent, dynamic variation of both voltage and frequency. Blackfin processors also employ a gated clock scheme and multiple power-down modes for minimal power consumption.

Ease of Use

Blackfin processors employ both an optimized compiler and architecture to support software development in HLL, for example, C/C++, thus delivering code densities comparable to those of traditional microcontrollers. The architecture also has embedded features to support efficient use of a real-time operating system (RTOS).

Features

- Up to 350 MHz/700 MMACS
- 16-bit dual-MAC processor core
- Flexible, software controlled dynamic power management
- Enhanced media instructions for audio, image, and video multimedia applications
- Integrated system peripherals, including USB device, PCI, serial ports, UARTs, SPI, and timers
- Core voltage: 0.95 V to 1.65 V

Blackfin Processors Utilize:

- Single processor core
- Single instruction set
- Single programming model
- Single set of development tools

Applications

- Automotive applications
- Broadband home gateways
- Central office/network switch
- Digital imaging and printing
- Global positioning systems
- Home networking/wireless LAN
- Internet appliances
- Modem solutions
- PDAs and other portable handheld devices
- Video conferencing
- VoIP phone solutions
- Personal branch exchanges (PBX)
- Point-of-sale terminals
- Telecommunications

Part Number	Max (MHz)	Max (MMACS)	L1/L2 Memory (kB)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-BF535PBB-200	200	400	52/256	−40 to +85		260-ball PBGA	
ADSP-BF535PBB-300	300	600	52/256	−40 to +85		260-ball PBGA	
ADSP-BF535PBBZ-200	200	400	52/256	−40 to +85		260-ball PBGA	
ADSP-BF535PKB-300	300	600	52/256	0 to 70	2 SPIs, 2 SPORTs, USB device, PCI	260-ball PBGA	31.27 to 48.22
ADSP-BF535PKB-350	350	700	52/256	0 to 70		260-ball PBGA	
ADSP-BF535PKBZ-300	300	600	52/256	0 to 70		260-ball PBGA	
ADSP-BF535PKBZ-350	350	700	52/256	0 to 70		260-ball PBGA	

NOTES
[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

SHARC Processor Family
Leadership in Floating-Point Applications

Analog Devices 32-bit floating-point SHARC processors are based on a Super Harvard Architecture that balances exceptional core and memory performance with outstanding I/O throughput capabilities. This Super Harvard Architecture extends the original concepts of separate program and data memory buses by adding an I/O processor with its associated dedicated buses. In addition to satisfying the demands of the most computationally intensive, real-time signal processing applications, SHARC processors integrate large memory arrays and application-specific peripherals designed to simplify product development and reduce time to market.

The SHARC processor portfolio currently consists of four generations of products providing code-compatible solutions ranging from entry-level to the high performance products offering fixed- and floating-point computational power. All SHARC processors provide a common set of features and functionality usable across many signal processing markets and applications, allowing designers an easy transition to the newest products with the latest features and the highest performance.

First Generation

First generation SHARC processors offer performance to 66 MHz/ 198 MFLOPS. Their easy to use instruction set architecture supports both 32-bit fixed-point and 32-/40-bit floating-point data formats combined with large memory arrays, and sophisticated communications ports make them suitable for a wide array of parallel processing applications, including consumer audio, medical imaging, military, industrial, and instrumentation.

Second Generation

Second generation SHARC processors double the level of signal processing performance (100 MHz/600 MFLOPS) by utilizing a single-instruction, multiple-data (SIMD) architecture. This hardware extension doubles the number of computational resources available to the system programmer. Second generation products contain dual multipliers, ALUs, shifters, and data register files—significantly increasing overall system performance. This capability is especially relevant in consumer, automotive, and professional audio applications where the algorithms related to multichannel processing can effectively utilize the SIMD architecture.

Third Generation

Third generation SHARC processors are based on an enhanced SIMD architecture, which extends core performance to an impressive 400 MHz/2.4 GFLOPS. Third generation SHARC audio processors feature a high level of integrated on-chip peripherals, such as multichannel audio surround sound decoders and postprocessing algorithms, S/PDIF transmitter/receiver, high performance asynchronous sample-rate conversion, PWM channels, code security, and DTCP cipher for protection of digital data in automobiles. A number of third generation processors are also pin-compatible for use with a single hardware platform.

Fourth Generation

Fourth generation SHARC processors not only increase the core performance to an industry-leading 450 MHz/2.7 GFLOPs but also boost the performance with the addition of accelerator logic to off-load core activities from being consumed by filter processing. Fourth generation SHARC processors integrate some of the highest memory on-chip RAM with a capacity of 5 Mb. Extra memory capacity is further enhanced with the innovative VISA (variable instruction set architecture) mode where programs can save up to 30% of code size by reducing the opcodes for many instructions. For industrial and automotive applications, fourth generation processors also incorporate a thermal diode to allow customers the flexibility to operate in higher ambient operating temperature conditions without sacrificing overall performance. DTCP cipher for protection of digital data in automotive applications is also integrated in automotive parts.

Integration of peripherals continues with serial ports, SPI ports, S/PDIF Tx/Rx, and an 8-channel asynchronous sample rate converter block. The fourth generation SHARC processor allows data from the serial ports to be directly transferred to external memory by the DMA controller, again preserving internal memory space for code and data. The fourth generation processor also incorporates link ports that allow processor to processor communication for data movement. Some fourth generation SHARC processors also integrate real-time clock (RTC) and watchdog timer functionality.

SHARC Processor Product Portfolio

Highest Performance →

	ADSP-21261 ADSP-21262	ADSP-21266	ADSP-21362 ADSP-21363¹ ADSP-21364¹	ADSP-21371 ADSP-21375	ADSP-21368 ADSP-21369	ADSP-21365 ADSP-21366¹ ADSP-21367	ADSP-21478 ADSP-21479	ADSP-21483 ADSP-21486 ADSP-21487 ADSP-21488 ADSP-21489	ADSP-21469	Future
Performance > 2 GFLOPS					•	•		•	•	•
Application-Specific Peripherals			•	•	•	•	•	•	•	•
Configurable Applications I/O Interface			•	•	•	•	•	•	•	
Low Cost	•		•				•	•		
Audio Decoders in ROM		•				•				
Hardware Accelerators			•		•	•	•	•	•	•
High Speed Interprocessor Communication (Link Ports)									•	
Low Power							•			

NOTES
¹ADSP-21363, ADSP-21364, ADSP-21366 do not have hardware accelerators.

Blue product number indicates automotive grade is available.

SHARC Processor Family
Leadership in Floating-Point Applications

All SHARC processors are code-compatible with previous generations of SHARC processors, so legacy code is easily ported to the newer products. In addition, a number of third generation processors are also pin-compatible for use with a single hardware platform.

- Home theater applications—The ADSP-21266, ADSP-21363, ADSP-21366, ADSP-21367, ADSP-21483, ADSP-21486, and ADSP-21487 permit highly efficient software implementations of audio decode and postprocessing algorithms, such as Dolby Digital, Dolby Digital EX, DTS-ES Discrete 6.1, DTS-ES Matrix 6.1, DTS 96/24™ 5.1, DTS-HD, DTS Express, MPEG-2 AAC LC, MPEG-2 BC 2ch, Dolby Pro Logic II, Dolby Pro Logic 2x, Dolby True HD, DTS Neo:6, DDPlus DCV, Neural Audio, Audyssey room equalization, and WMA Pro. Libraries of all standard—and many proprietary—audio algorithms reside in on-chip ROM, eliminating the need for external ROM.

- Professional audio applications—A number of the third generation (ADSP-2136x) and fourth generation (ADSP-2146x) SHARC processors are well-suited for professional audio applications requiring high processing power and advanced on-chip peripherals such as sample rate conversion, S/PDIF transmitter/receiver, and BGA and LQFP package options.

- Broad market use—SHARC processors are available in commercial, industrial, and automotive temperature grade packages. They are used in a wide variety of signal processing applications, providing up to 450 MHz performance in a single instruction, multiple data (SIMD) architecture.

The combination of a high performance core surrounded by appropriate peripherals, a large software library, and award-winning CROSSCORE development tools makes the third generation SHARC processors the ideal choice for audio and broad market processor applications.

SHARC Melody Platform

Analog Devices' SHARC Melody platform brings the highest quality audio processing available to audio receivers based on the premium performance of the third generation SHARC processors. The SHARC Melody with floating-point capability provides the highest quality platform on which to build high fidelity audio decoders and is now widely available in home theater systems designed by a range of leading global brands. These programmable DSP-based platforms ensure that end equipment is always up to date and able to support the newest standards as soon as content is available.

Music enthusiasts love the quality of their living room surround sound systems. These audiophiles want that experience in their cars, necessitating a variety of audio-spatializer algorithms and equalizer functions that can be developed on SHARC Melody platforms. For midrange systems required in cars, Analog Devices also offers a SigmaDSP that integrates 24-bit DSP functionality with very high performance digital-to-analog converters to make an integrated, customizable equalizer.

ADI also offers a wide range of audio codec and amplifier components, plus software to support in-car music playing and recording.

Part Number	Clock Speeds MHz	32-Bit Floating Point MMACS	On Chip L1 SRAM (Bits)	On Chip ROM (Bits)	External Memory Type Supported	DMA (Channels)	Serial Ports	Other Ports/Features	Number of GPIOs	Timers	Core V_{DDINT} (Max Speed)	External (I/O)	Total Core Power Max (mW)	Package[4,5]	Temperature Range (Non-automotive Grade)	Temperature Range Automotive Grade (W)	Price @ 1k (U.S.)[6]	Availability
ADSP-21488[7]	300	600	3M	4M	—	32	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, FIR/IIR/FFT accelerator	Up to 9	2 GPs	1.10	3.3	635	14 mm × 14 mm, 0.5 mm, 100-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C	8.54	
	350	700									1.10		682				9.96	Production
	400	800									1.10		728				11.36	
	300	600			Async; 16-bit SDRAM	34				2 GP WDTs	1.10		635	24 × 24 mm, 0.5 mm, 176-lead LQFP_EP			9.49	
	350	700									1.10		682				11.07	
	400	800									1.10		728				12.62	
ADSP-21489[7]	300	600	5M	4M	—	32	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, FIR/IIR/FFT accelerator	Up to 9	2 GPs	1.10	3.3	635	14 mm × 14 mm, 0.5 mm, 100-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C	12.86	
	350	700									1.10		682				14.29	Production
	400	800									1.10		728				17.86	
	300	600			Async; 16-bit SDRAM	34				2 GP WDTs	1.10		635	24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP			14.29	
	350	700									1.10		682				15.88	
	400	800									1.10		728				19.85	
ADSP-21478[7]	200	400	3M	4M	—	32	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, shift register, FIR/IIR/FFT accelerator	Up to 9	2 GP WDTs	1.20	3.3	150	14 mm × 14 mm, 0.5 mm, 100-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +105°C	7.99	
	266	532									1.20		250			−40°C to +105°C	8.51	Production
	200	400			Async; 16-bit SDRAM	34				2 GP WDT RTCs	1.20		150	12 mm × 12 mm, 0.8 mm, 196-ball CSP_BGA		−40°C to +85°C	8.33	
	266	532									1.20		250			−40°C to +85°C	9.25	
ADSP-21479[7]	200	400	5M	4M	—	32	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, shift register, FIR/IIR/FFT accelerator	Up to 9	2 GP WDTs	1.20	3.3	150	14 mm × 14 mm, 0.5 mm, 100-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +105°C	8.81	
	266	532									1.20		250			−40°C to +105°C	9.79	Production
	200	400			Async; 16-bit SDRAM	34				2 GP WDT RTCs	1.20		150	12 mm × 12 mm, 0.8 mm, 196-ball CSP_BGA		−40°C to +85°C	9.04	
	266	532									1.20		250			−40°C to +85°C	10.64	
ADSP-21469[7]	400	800	5M	4M	Async; 16-bit DDR2	36	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, PWM, 4 PCGs, 2 link ports, FIR/IIR/FFT accelerator	Up to 8	3 GPs	1.05	3.3 1.8 (DDR2)	617	19 mm × 19 mm, 1.0 mm, 324-ball CSP_BGA	−40°C to +85°C, 0°C to +70°C	Contact ADI	28.50	Production
	450	900									1.10		773		0°C to +70°C		31.50	
ADSP-21371	200	400	1M	4M	Async; 32-bit SDRAM	32	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, PWM, 4 PCGs	Up to 16	2 GPs	1.00	3.3	400	28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP	0°C to +70°C	−40°C to +105°C	13.27	Production
	266	532									1.20		720		−40°C to +85°C, 0°C to +70°C	−40°C to +85°C	13.27	
ADSP-21375	200	400	0.5M	2M	Async; 16-bit SDRAM	24	4 SPORTs, 2 SPIs, UART, TWI	PWM, 4 PCGs	Up to 16	3 GPs	1.00	3.3	400	28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP	—	−40°C to +105°C	Contact ADI	Production
	266	532									1.20		720		−40°C to +85°C, 0°C to +70°C	−40°C to +85°C	9.83	
ADSP-21368	333	666	2M	6M	Async; 32-bit SDRAM	34	8 SPORTs, 2 SPIs, 2 UARTs, TWI	S/PDIF, ASRC, PWM, 4 PCGs, shared external memory	Up to 16	3 GPs	1.20	3.3	1080	27 mm × 27 mm, 1.27 mm, 256-ball SBGA	−40°C to +85°C, 0°C to +70°C	—	31.04	Production
	400	800									1.30		1430		0°C to +70°C		41.39	
ADSP-21369	266	532	2M	6M	Async; 32-bit SDRAM	34	8 SPORTs, 2 SPIs, 2 UARTs, TWI	S/PDIF, ASRC, PWM, 4 PCGs	Up to 16	3 GPs	1.20	3.3	840	28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C	19.69	
	333	666									1.20		1080	27 mm × 27 mm, 1.27 mm, 256-ball SBGA, 28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP			22.65	Production
	350	700									1.30		1365	28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP, 27 mm × 27 mm, 1.27 mm, 256-ball SBGA	0°C to +70°C	—	26.05	
	366	732									1.30		1404				27.35	
	400	800									1.30		1430	27 mm × 27 mm, 1.27 mm, 256-ball SBGA			32.81	
ADSP-21362	200	400	3M	4M	Async	25	6 SPORTs, 2 SPIs	S/PDIF, ASRC, PWM, 2 PCGs	Up to 16	3 GPs	1.00	3.3	800	20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +105°C	−40°C to +105°C	32.55	Production
	333	666									1.20		960	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA, 20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C (BGA only)	27.12	
ADSP-21363	200	400	3M	4M	Async	25	6 SPORTs, 2 SPIs	PWM, 2 PCG	Up to 16	3 GPs	1.00	3.3	800	20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +105°C	−40°C to +105°C	29.13	Production
	333	666									1.20		960	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA, 20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C (BGA only)	20.22	
ADSP-21364	200	400	3M	4M	Async	25	6 SPORTs, 2 SPIs	S/PDIF, ASRC, PWM, 2 PCGs	Up to 16	3 GPs	1.00	3.3	800	20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +105°C	−40°C to +105°C	42.85	Production
	333	666									1.20		960	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA, 20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C (BGA only)	29.75	
ADSP-21261	150	300	1M	3M	Async	18	4 SPORTs, SPI	2 PCGs	Up to 16	3 GPs	1.20	3.3	<600	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA, 20 mm × 20 mm, 0.5 mm, 144-lead LQFP	0°C to +70°C	−40°C to +85°C	6.64	Production
ADSP-21262	150	300	2M	4M	Async	22	6 SPORTs, SPI	2 PCGs	Up to 16	3 GPs	1.20	3.3	<600	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA	−40°C to +85°C	−	21.94	Production
	200	400									1.20		600	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA 20 mm × 20 mm, 0.5 mm, 144-lead LQFP	0°C to +70°C		17.15	

SHARC Audio Processors (include audio-specific peripherals and on-chip factory-programmed ROM. License agreement required from IP holders.)

Part Number	Performance		Memory			DMA (Channels)	Peripheral Options[1]				Voltage (V) Nominal[2]		Total Core Power Max (mW)[3]	Packaging and Operating Temperature Range Options[4,5]			Price @ 1k ($U.S.)[6]	Availability
	Clock Speeds MHz	32-Bit Floating Point MMACS	On Chip L1 SRAM (Bits)	On Chip ROM (Bits)	External Memory Type Supported		Serial Ports	Other Ports/Features	Number of GPIOs	Timers	Core V$_{nom}$ (Max Speed)	External (I/O)		Package[4,5]	Temperature Range (Non-automotive Grade)	Temperature Range Automotive Grade (W)[2]		
ADSP-21483	350	700	3M	Audio decoders	Async, 16-bit SDRAM	34	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, FIR/IIR/FFT accelerator	Up to 9	2 GPs	1.00[8]	3.3	586[6]	24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP	0°C to +70°C	—		Production
	400	800									1.00[8]		617[7]			—		
ADSP-21486	350	700	5M	Audio decoders	—	32	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, FIR/IIR/FFT accelerator	Up to 9	2 GPs	1.00[8]	3.3	586[6]	14 mm × 14 mm, 0.5 mm, 100-lead LQFP_EP	0°C to +70°C	—		Production
	400	800									1.00[8]		617[7]					
	350	700			Async						1.00[8]		586[6]	24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP				
	400	800									1.00[8]		617[7]					
ADSP-21487	350	700	5M	Audio decoders	Async, 16-bit SDRAM	34	8 SPORTs, 2 SPIs, UART, TWI	S/PDIF, ASRC, 4 PWMs, 4 PCGs, FIR/IIR/FFT accelerator	Up to 9	2 GPs	1.00[8]	3.3	586[6]	24 mm × 24 mm, 0.5 mm, 176-lead LQFP_EP	0°C to +70°C	—		Production
	400	800									1.00[8]		617[7]			—		
ADSP-21365	200	400	3M	Audio decoders	Async	25	6 SPORTs, 2 SPIs	S/PDIF, ASRC, PWM, 2 PCGs	Up to 16	3 GPs	1.00	3.3	800	20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +105°C	−40°C to +105°C		Production
	333	666									1.20		960	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA; 20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +85°C	−40°C to +85°C (BGA only)		
ADSP-21366	200	400	3M	Audio decoders	Async	25	6 SPORTs, 2 SPIs	S/PDIF, ASRC, PWM, 2 PCGs	Up to 16	3 GPs	1.00	3.3	800	20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +105°C	−40°C to +105°C	Contact ADI	Production
	333	666									1.20		960	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA; 20 mm × 20 mm, 0.5 mm, 144-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	−40°C to +85°C (BGA only)		
ADSP-21367	266	532	2M	Audio decoders	Async, 32-bit SDRAM	34	8 SPORTs, 2 SPIs, 2 UARTs, TWI	S/PDIF, ASRC, PWM, 4 PCGs	Up to 16	3 GPs	1.20	3.3	840	28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP	−40°C to +85°C, 0°C to +70°C	—		Production
	333	666									1.20		1080	27 mm × 27 mm, 1.27 mm, 256-ball SBGA; 28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP				
	350	700									1.30		1365	28 mm × 28 mm, 0.5 mm, 208-lead LQFP_EP	0°C to +70°C			
	366	732									1.30		1404					
	400	800									1.30		1430	27 mm × 27 mm 1.27 mm, 256-ball SBGA				
ADSP-21266	150	300	2M	Audio decoders	Async	22	6 SPORTs, SPI	PWM, 2 PCGs	Up to 16	3 GPs	1.20	3.3	<600	12 mm × 12 mm, 0.8 mm, 136-ball CSP_BGA; 20 mm × 20 mm, 0.5 mm, 144-lead LQFP	0°C to +70°C	—		Production
	200	400									1.20		600					

NOTES

[1] Due to pin muxing options, not all peripheral combinations maybe available together—please refer to data sheet and user manuals for full information.

[2] Automotive grade products may require different voltage conditions—please refer to data sheet for full information.

[3] Core Power (mW) stated for max core operating speed of the device at TA = 25°C, ASF = 1.0 (V$_{DDINT}$ nominal, I$_{DD-INTYP}$ supply current. Typical activity is the core executing a multifunction instruction fetched from internal memory, with 4 core memory accesses per CLKIN cycle (DMx64) and DMA through 3 SPORTs running. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random). Please refer to associated data sheet and EE notes for further details and complete power calculation information. Dynamic power management available via software programmable PLL.

[4] All DSP products available in RoHS compliant options—please refer to data sheet for complete information

[5] All packaging, operating temperature and grade combinations may not be available—please refer to data sheet for full information and contact ADI for options outside those listed.

[6] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate the lowest priced version of that particular speed device and will vary depending on package type and/or temperature range and grade.

[7] Also available with an automotive grade (with DTCP and MLB options).

[8] Pricing, power, and core voltage are subject to change—please contact ADI for further information.

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489 SHARC Processors
High Performance Fourth Generation DSP

The fourth generation of SHARC processors now includes the ADSP-2148x family and offers increased performance, hardware-based filter accelerators, audio and application-focused peripherals, and new memory configurations capable of supporting the latest surround-sound decoder algorithms. All devices are pin-compatible with each other and completely code-compatible with all prior SHARC processors. These newest members of the fourth generation SHARC processor family are based on a single-instruction, multiple-data (SIMD) core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats making them particularly suitable for high performance audio applications.

The ADSP-2148x processor series offers the highest performance—400 MHz/2400 MFLOPs—in an LQFP package and includes additional processing blocks such as FIR, IIR, and FFT accelerators to increase the total performance of the system. There is a new feature called variable instruction set architecture (VISA) that allows the code size to be decreased by 20% to 30% and increase the memory size availability. The fourth generation DSP allows the ability to connect to external memory by providing a glueless interface to 16-bit wide SDR SDRAMs.

Fourth generation SHARC processors also integrate application-specific peripherals designed to simplify hardware design, minimize design risks, and ultimately reduce time to market. Grouped together, and broadly named the digital applications interface (DAI), these functional blocks may be connected to each other or to external pins via the software-programmable signal routing unit (SRU). The SRU is an innovative architectural feature that enables complete and flexible routing amongst DAI blocks. Peripherals connected through the SRU include but are not limited to serial ports, IDP, S/PDIF Tx/Rx, and an 8-channel asynchronous sample rate converter block. The fourth generation SHARC processor allows data from the serial ports to be directly transferred to external memory by the DMA controller. Other peripherals such as SPI, UART and 2-wire interface are routed through a digital peripheral interface (DPI).

Features

- 400 MHz core clock speed
- 3 Mbits or 5 Mbits of on-chip RAM
- FIR, IIR, and FFT accelerators
- 16-bit wide SDR SDRAM external memory interface
- Digital applications interface (DAI) enabling user-definable access to peripherals including an S/PDIF Tx/Rx, and 8-channel asynchronous sample rate converter
- Fully enhanced DMA engine including scatter/gather DMA, delay line DMA
- 8 serial ports (SPORTs) supporting I²S, left-justified sample pair, DSP serial, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- UART and 2-wire interface
- 16 pulse width modulation (PWM) channels
- 3 full-featured timers
- 176-lead LQFP E-Pad and 100-lead LQFP E-Pad packages
- Commercial and industrial temperature ranges

Applications

- Industrial control
- Automotive audio
- Medical applications

ADSP-2148x Block Diagram
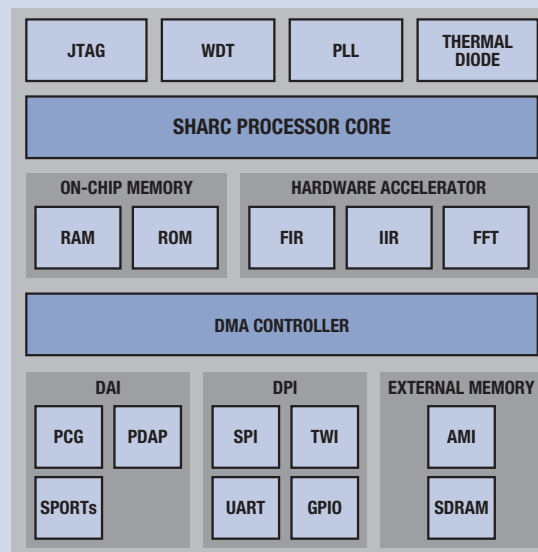
ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489 SHARC Processors
High Performance Fourth Generation DSP

Part Number[1]	Speed (MHz)	On-Chip Memory SRAM/ROM (Mb)	Temperature Range	Key Peripherals	Package	Price Range @1k ($U.S.)[2,3]
ADSP-21483KSWZ-3B	350	3/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21483KSWZ-4B	400	3/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21486KSWZ-3A	350	5/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21486KSWZ-3B	350	5/4	0°C to 70°C		176-lead LQFP E-Pad	Contact ADI
ADSP-21486KSWZ-4A	400	5/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21486KSWZ-4B	400	5/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21487KSWZ-3B	350	5/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21487KSWZ-4B	400	5/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21488BSWZ-2A	300	3/4	−40°C to 85°C	2 timers, 1 UART, 8 SPORTs, 8-channel ASRC, 2 SPIs, 1 TWI, 4 PCGs, PWM, S/PDIF Rx/Tx Integrated audio decoders (ADSP-21483/ ADSP-21487 only)	100-lead LQFP E-Pad	
ADSP-21488BSWZ-2B	300	3/4	−40°C to 85°C		176-lead LQFP E-Pad	
ADSP-21488BSWZ-3A	350	3/4	−40°C to 85°C		100-lead LQFP E-Pad	
ADSP-21488BSWZ-3B	350	3/4	−40°C to 85°C		176-lead LQFP E-Pad	
ADSP-21488BSWZ-4A	400	3/4	−40°C to 85°C		100-lead LQFP E-Pad	8.54 to 18.35
ADSP-21488BSWZ-4B	400	3/4	−40°C to 85°C		176-lead LQFP E-Pad	
ADSP-21488KSWZ-2A	300	3/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21488KSWZ-2B	300	3/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21488KSWZ-3A	350	3/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21488KSWZ-3B	350	3/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21488KSWZ-4A	400	3/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21488KSWZ-4B	400	3/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21489BSWZ-2A	300	5/4	−40°C to 85°C		100-lead LQFP E-Pad	
ADSP-21489BSWZ-2B	300	5/4	−40°C to 85°C		176-lead LQFP E-Pad	
ADSP-21489BSWZ-3A	350	5/4	−40°C to 85°C		100-lead LQFP E-Pad	
ADSP-21489BSWZ-3B	350	5/4	−40°C to 85°C		176-lead LQFP E-Pad	
ADSP-21489BSWZ-4A	400	5/4	−40°C to 85°C		100-lead LQFP E-Pad	
ADSP-21489BSWZ-4B	400	5/4	−40°C to 85°C		176-lead LQFP E-Pad	12.86 to 23.81
ADSP-21489KSWZ-2A	300	5/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21489KSWZ-2B	300	5/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21489KSWZ-3A	350	5/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21489KSWZ-3B	350	5/4	0°C to 70°C		176-lead LQFP E-Pad	
ADSP-21489KSWZ-4A	400	5/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21489KSWZ-4B	400	5/4	0°C to 70°C		176-lead LQFP E-Pad	

[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

[3] Pricing is subject to change. Please contact ADI for further information.

Z = RoHS compliant part.

License agreement required from IP holders before purchase of the ADSP-21483, ADSP-21486, and ADSP-21487.

ADSP-21478/ADSP-21479 SHARC Processors
High Performance Fourth Generation DSP

The fourth generation of SHARC processors now includes the low power floating-point DSP products—the ADSP-21478 and ADSP-21479—and offers increased performance, hardware-based filter accelerators, audio and application-focused peripherals, and new memory configurations capable of supporting a single chip solution. All devices are pin-compatible with each other and completely code-compatible with all prior SHARC processors. These newest members of the fourth generation SHARC processor family are based on a single-instruction, multiple-data (SIMD) core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats and their low power make them particularly suitable for battery powered applications or where a higher ambient operating temperature is required.

The ADSP-2147x series offers very low power and high performance— 266 MHz/1596 MFLOPs—in a BGA and LQFP package. This feature of power makes the ADSP-2147x processors particularly well suited to address the automotive audio and many industrial control segments where low power is a requirement. In addition to its high core performance, the ADSP-21479 includes additional processing blocks such as FIR, IIR, and FFT accelerators to increase the total performance of the system. There is a new feature called variable instruction set architecture (VISA) that allows the code size to be decreased by 20% to 30% and increase the memory size availability. The fourth generation DSP allows the ability to connect to external memory by providing a glueless interface to 16-bit wide SDR SDRAMs.

Fourth generation SHARC processors also integrate application-specific peripherals designed to simplify hardware design, minimize design risks, and ultimately reduce time to market. Grouped together, and broadly named the digital applications interface (DAI), these functional blocks may be connected to each other or to external pins via the software-programmable signal routing unit (SRU). The SRU is an innovative architectural feature that enables complete and flexible routing amongst DAI blocks. Peripherals connected through the SRU include but are not limited to serial ports, IDP, S/PDIF Tx/Rx, and an 8-channel asynchronous sample rate converter block. The fourth generation SHARC processor allows data from the serial ports to be directly transferred to external memory by the DMA controller. Other peripherals such as SPI, UART and 2-wire interface are routed through a digital peripheral interface (DPI).

Features

- 266 MHz core clock speed
- 3 Mbits or 5 Mbits of on-chip RAM
- FIR, IIR, and FFT accelerators
- 16-bit wide SDR SDRAM external memory interface
- Digital applications interface (DAI) enabling user-definable access to peripherals including an S/PDIF Tx/Rx, and 8-channel asynchronous sample rate converter
- Fully enhanced DMA engine including scatter/gather DMA, delay line DMA
- Real-time clock (RTC)
- 8 serial ports (SPORTs) supporting I²S, left-justified sample pair, and TDM modes
- Watchdog timer
- Shift registers
- 2 SPI-compatible ports supporting master and slave modes
- UART and 2-wire interface
- 16 pulse width modulation (PWM) channels
- 3 full-featured timers
- 196-ball CSP_BGA and 100-lead LQFP E-Pad packages
- Commercial, industrial, and automotive temperature ranges

Applications

- Industrial control and instrumentation
- Automotive audio
- Medical applications

ADSP-21478/ADSP-21479 Block Diagram
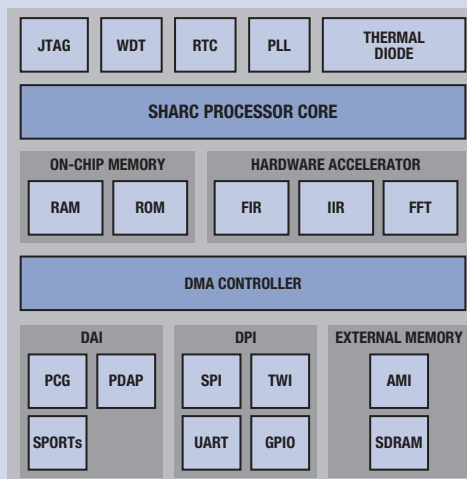
ADSP-21478/ADSP-21479 SHARC Processors
High Performance Fourth Generation DSP

Part Number[1]	Speed (MHz)	On-Chip Memory SRAM/ROM (Mb)	Temp Range	Key Peripherals	Package	Price Range @1k ($U.S.)[2,3]
ADSP-21478BBCZ-1B	200	3/4	−40°C to +85°C		196-ball CSP_BGA	
ADSP-21478BBCZ-2B	266	3/4	−40°C to +85°C		196-ball CSP_BGA	
ADSP-21478BSWZ-1A	200	3/4	−40°C to +85°C		100-lead LQFP E-Pad	
ADSP-21478BSWZ-2A	266	3/4	−40°C to +85°C		100-lead LQFP E-Pad	7.99 to 11.10
ADSP-21478KBCZ-1B	200	3/4	0°C to 70°C		196-ball CSP_BGA	
ADSP-21478KBCZ-2B	266	3/4	0°C to 70°C	2 timers, 1 UART,	196-ball CSP_BGA	
ADSP-21478KSWZ-1A	200	3/4	0°C to 70°C	8 SPORTs,	100-lead LQFP E-Pad	
ADSP-21478KSWZ-2A	266	3/4	0°C to 70°C	8-channel ASRC, 2 SPIs,	100-lead LQFP E-Pad	
ADSP-21479BBCZ-1B	200	5/4	−40°C to +85°C	1 TWI, 4 PCGs,	196-ball CSP_BGA	
ADSP-21479BBCZ-2B	266	5/4	−40°C to +85°C	PWM, S/PDIF Rx/Tx, WDT	196-ball CSP_BGA	
ADSP-21479BSWZ-1A	200	5/4	−40°C to +85°C		100-lead LQFP E-Pad	
ADSP-21479BSWZ-2A	266	5/4	−40°C to +85°C	RTC (196 BGA only)	100-lead LQFP E-Pad	8.81 to 12.71
ADSP-21479KBCZ-1B	200	5/4	0°C to 70°C		196-ball CSP_BGA	
ADSP-21479KBCZ-2B	266	5/4	0°C to 70°C		196-ball CSP_BGA	
ADSP-21479KSWZ-1A	200	5/4	0°C to 70°C		100-lead LQFP E-Pad	
ADSP-21479KSWZ-2A	266	5/4	0°C to 70°C		100-lead LQFP E-Pad	

NOTES

[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

[3] Pricing is subject to change. Please contact ADI for further information.

Z = RoHS compliant part.

ADSP-21469 SHARC Processors
High Performance Fourth Generation Processors

The fourth generation of SHARC processors, which includes the ADSP-21469, offers increased performance, hardware-based filter accelerators, audio and application-focused peripherals, and new memory configurations capable of supporting the latest surround-sound decoder algorithms. All devices are pin-compatible with each other and completely code-compatible with all prior SHARC processors. These newest members of the SHARC processor family are based on a single-instruction, multiple-data (SIMD) core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats, making them particularly suitable for high performance audio applications.

There is a new feature called variable instruction set architecture (VISA) that allows the code size to be decreased by 20% to 30% and increases the memory size availability. The fourth generation SHARC processors allow the ability to connect to faster external memory by providing a glueless interface to DDR2 SDRAMs.

Fourth generation SHARC processors also integrate application-specific peripherals designed to simplify hardware design, minimize design risks, and ultimately reduce time to market. Grouped together, and broadly named the digital applications interface (DAI), these functional blocks can be connected to each other or to external pins via the software-programmable signal routing unit (SRU). The SRU is an innovative architectural feature that enables complete and flexible routing among DAI blocks. Peripherals connected through the SRU include but are not limited to serial ports, SPI ports, S/PDIF Tx/Rx, and an 8-channel asynchronous sample rate converter block. The fourth generation SHARC processors allow data from the serial ports to be directly transferred to external memory by the DMA controller. Other peripherals such as UART and 2-wire interface are routed through a digital peripheral interface (DPI).
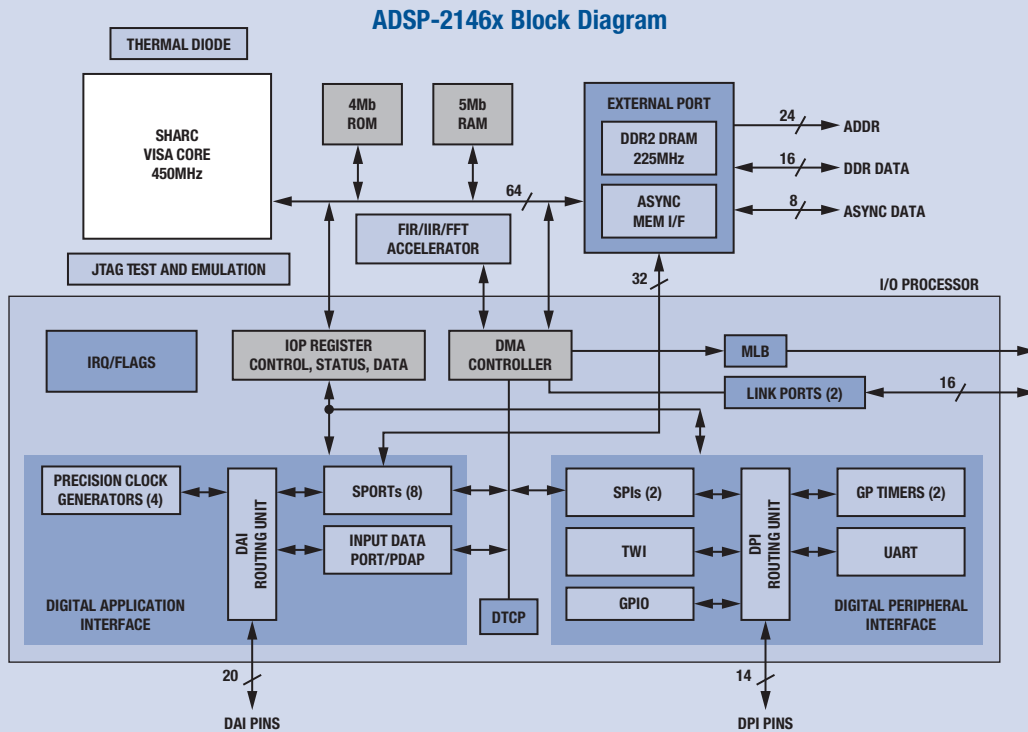
Features

- 450 MHz core clock speed
- 5 Mb of on-chip RAM
- 4 Mb of on-chip ROM
- FIR, IIR, and FFT accelerators
- 16-bit wide DDR2 external memory interface
- Digital applications interface (DAI) enabling user-definable access to peripherals, including an S/PDIF Tx/Rx and 8-channel asynchronous sample rate converter
- Fully enhanced DMA engine including scatter/gather DMA, delay line DMA
- 2 link ports
- 8 serial ports (SPORTs) supporting I²S, left-justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- UART and 2-wire Interface
- 16 pulse width modulation (PWM) channels
- 3 full-featured timers
- 324-ball PBGA package
- Commercial and industrial temperature ranges
- Core voltage: 1.0 V to 1.1 V

Applications

- Industrial control
- Professional audio
- Medical applications
- Automotive audio
- Professional audio
- Consumer AVR
- Digital audio amplifiers

ADSP-21469 SHARC Processors
High Performance Fourth Generation Processors

ADSP-2146x Block Diagram

Part Number[1]	Speed (MHz)	On-Chip Memory SRAM/ROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @1k ($U.S.)[2, 3]
ADSP-21469BBCZ-3	400	5/4	−40 to +85	2 timers, 1 UART, 8 SPORTs, 8-channel ASRC, 2 SPIs, 16-bit DDR2 interface, 1 TWI, 4 PCGs, PWM, S/PDIF Rx/Tx, DAI, DPI, link ports, integrated audio decoders (ADSP-21467 only)	324-ball CSP_BGA	28.50 to 37.80[3]
ADSP-21469KBCZ-3	400	5/4	0 to 70		324-ball CSP_BGA	
ADSP-21469KBCZ-4	450	5/4	0 to 70		324-ball CSP_BGA	

NOTES

[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

[3] Pricing is subject to change. Please contact ADI for further information.

Z = RoHS compliant part.

ADSP-21371/ADSP-21375 SHARC Processors
High Performance 32-Bit Floating-Point Processors

The ADSP-21371 and the ADSP-21375 provide the highest MFLOPS/$ performance for a variety of applications. Both the ADSP-21371 and the ADSP-21375 devices are pin-compatible and code-compatible with prior SHARC processors such as the ADSP-21367 and ADSP-21369. These members of the SHARC processor family are based on a single-instruction, multiple-data (SIMD) core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats, making them particularly suitable for cost optimized high precision applications.

The ADSP-2137x SHARC processors also integrate many peripherals designed to simplify hardware design, minimize system design risks, and reduce end-customer time to market. Grouped together, and broadly named the digital applications interface (DAI), these functional blocks can be connected to each other or to external pins via the software-programmable signal routing unit (SRU). The SRU is an innovative architectural feature that enables complete and flexible routing among DAI blocks. Peripherals connected through the SRU include, but are not limited to, serial port and SPI port blocks.

The ADSP-21375 provides up to 266 MHz core clock performance with 0.5 Mb on-chip SRAM and four serial ports. The ADSP-21371 provides the same maximum core clock frequency with 1.0 Mb on-chip SRAM and eight serial ports.

Features

- 266 MHz SIMD SHARC core, capable of 1596 MFLOPS peak performance
- 0.5 Mb or 1.0 Mb SRAM
- 24 or 32 zero-overhead DMA channels
- Digital applications interface (DAI) enabling user-definable access to peripherals
- 4 or 8 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- 1 UART
- 1 TWI
- 2 full-featured timers
- 208-lead LQFP E-Pad package
- Commercial and industrial temperature ranges
- Core voltage: 1.2 V

Applications

- Professional audio
- Medical applications
- Industrial and instrumentation

ADSP-21371 Block Diagram
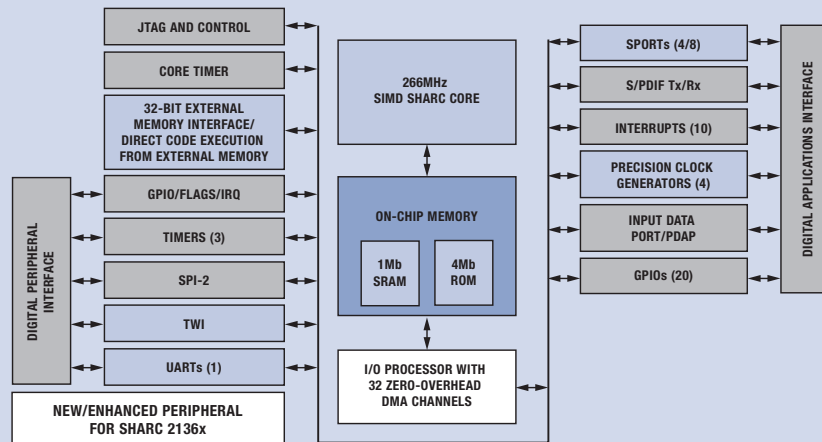
Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21371BSWZ-2B	266	1	−40 to +85	2 timers, 1 UART, 4 SPORTs, 2 SPIs, 1 TWI, 4 PCGs, PWM, DAI, 16-bit SDRAM interface	208-lead LQFP E-Pad	13.27 to 15.92
ADSP-21371KSWZ-2A	266	1	0 to 70		208-lead LQFP E-Pad	
ADSP-21371KSWZ-2B	266	1	0 to 70		208-lead LQFP E-Pad	
ADSP-21375BSWZ-2B	266	0.5	−40 to +85		208-lead LQFP E-Pad	9.83 to 11.79
ADSP-21375KSWZ-2B	266	0.5	0 to 70		208-lead LQFP E-Pad	

NOTES
[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processors
Industry-Leading Performance for Floating-Point Applications

The ADSP-21367/ADSP-21368/ADSP-21369, at speeds up to 400 MHz/ 2.4 GFLOPS, deliver superior performance and a high degree of functional integration. These floating-point SHARC processors are designed to simplify audio product development, reduce time to market, and reduce product costs for a variety of applications, including multichannel A/V receivers, professional mixing consoles, and digital synthesizers. Using these SHARC processors, manufacturers can create differentiated products for their customers more quickly, more easily, and more cost-effectively than ever before.

With its 6 Mb on-chip ROM factory-programmed with industry-standard audio decoders and postprocessor algorithms from Dolby, DTS, Microsoft, and SRS, the ADSP-21367 is one of the industry's high performers in audio processors available today.

The 400 MHz ADSP-21368 adds shared memory capabilities, making it an ideal choice for professional audio applications and other processing intensive applications.

The ADSP-21369 provides high performance signal processing with audio and broad market peripherals, as well as a 32-bit external memory interface supporting SRAM, SDRAM, flash, and ROM memory. Along with the ADSP-21367 and ADSP-21368, the ADSP-21369 supports both 16-bit and 32-bit SDRAM at speeds up to 166 MHz. The ADSP-21369 is well-suited to address the needs of professional audio applications and other applications where high performance processing is essential.

Features
- 400 MHz/2.4 GFLOPS SIMD SHARC core supporting 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 2 Mb SRAM, 6 Mb factory-programmed ROM (ADSP-21367 only)
- 32-bit external memory interface supports SDRAM, SRAM, flash, and ROM memory
- 8-channel, asynchronous sample rate conversion based on the AD1896
- S/PDIF transmitter and receiver
- 8 serial ports
- 2 precision clock generators
- 20 lines of digital I/O port
- 4 timers, UART, I²C-compatible interface
- ROM/JTAG security mode
- Available in 256-ball SBGA and 208-lead LQFP E-Pad package options
- Available in commercial and industrial temperature grades
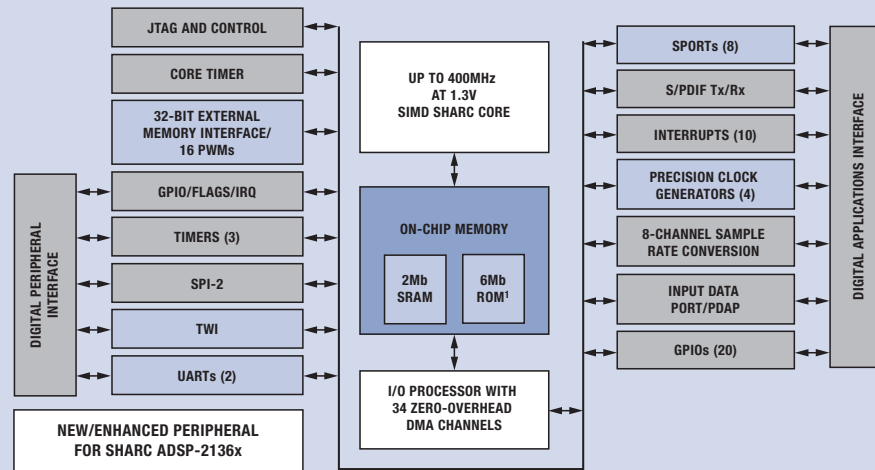- Core voltage: 1.2 V to 1.3 V

Applications
- Consumer A/V receivers
- Home theater systems
- Professional audio equipment
- Industrial and instrumentation

ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processors
Industry-Leading Performance for Floating-Point Applications

ADSP-21368/ADSP-21369 Block Diagram

[1] FOR CONSUMER APPLICATIONS

Part Number	Max (MHz)	On-Chip Memory SRAM/ROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21367BBP-2A	333	2/6	−40 to +85		256-ball SBGA	
ADSP-21367BBPZ-2A	333	2/6	−40 to +85		256-ball SBGA	
ADSP-21367BSWZ-1A	266	2/6	−40 to +85		208-lead LQFP E-Pad	
ADSP-21367KBP-2A	333	2/6	0 to 70		256-ball SBGA	
ADSP-21367KBPZ-2A	333	2/6	0 to 70		256-ball SBGA	Contact ADI
ADSP-21367KBPZ-3A	400	2/6	0 to 70		256-ball SBGA	
ADSP-21367KSWZ-1A	266	2/6	0 to 70		208-lead LQFP E-Pad	
ADSP-21367KSWZ-2A	333	2/6	0 to 70	3 timers, 2 UARTs,	208-lead LQFP E-Pad	
ADSP-21367KSWZ-4A	350	2/6	0 to 70	8 SPORTs, 2 SPIs,	208-lead LQFP E-Pad	
ADSP-21367KSWZ-5A	366	2/6	0 to 70	1 TWI, S/PDIF Rx/Tx,	208-lead LQFP E-Pad	
ADSP-21368BBP-2A	333	2/6	−40 to +85	4 PCGs, PWM, 8-channel	256-ball SBGA	
ADSP-21368BBPZ-2A	333	2/6	−40 to +85	ASRC, 32-bit SDRAM	256-ball SBGA	
ADSP-21368KBP-2A	333	2/6	0 to 70	interface, shared	256-ball SBGA	31.04 to 47.81
ADSP-21368KBPZ-2A	333	2/6	0 to 70	external memory support	256-ball SBGA	
ADSP-21368KBPZ-3A	400	2/6	0 to 70	(ADSP-21368 only),	256-ball SBGA	
ADSP-21369BBP-2A	333	2/6	−40 to +85	integrated audio	256-ball SBGA	
ADSP-21369BBPZ-2A	333	2/6	−40 to +85	decoders in ROM	256-ball SBGA	
ADSP-21369BSWZ-1A	266	2/6	−40 to +85	(ADSP-21367 only)	208-lead LQFP E-Pad	
ADSP-21369BSWZ-2A	333	2/6	−40 to +85		208-lead LQFP E-Pad	
ADSP-21369KBP-2A	333	2/6	0 to 70		256-ball SBGA	
ADSP-21369KBPZ-2A	333	2/6	0 to 70		256-ball SBGA	19.69 to 37.91
ADSP-21369KBPZ-3A	400	2/6	0 to 70		256-ball SBGA	
ADSP-21369KSWZ-1A	266	2/6	0 to 70		208-lead LQFP E-Pad	
ADSP-21369KSWZ-2A	333	2/6	0 to 70		208-lead LQFP E-Pad	
ADSP-21369KSWZ-4A	350	2/6	0 to 70		208-lead LQFP E-Pad	
ADSP-21369KSWZ-5A	366	2/6	0 to 70		208-lead LQFP E-Pad	

NOTES
[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.
License agreement required from IP holders before purchase of the ADSP-21367.

ADSP-21366 SHARC Processor
333 MHz Performance for Home Theater

The ADSP-21366 is particularly well-suited to address the increasing requirements of the professional audio and home theater market segments. In addition to its higher core performance, the ADSP-21366 includes peripherals such as 16-bit parallel ports, an S/PDIF transmitter/receiver, and an 8-channel asynchronous sample rate converter.

ADSP-21366 Block Diagram
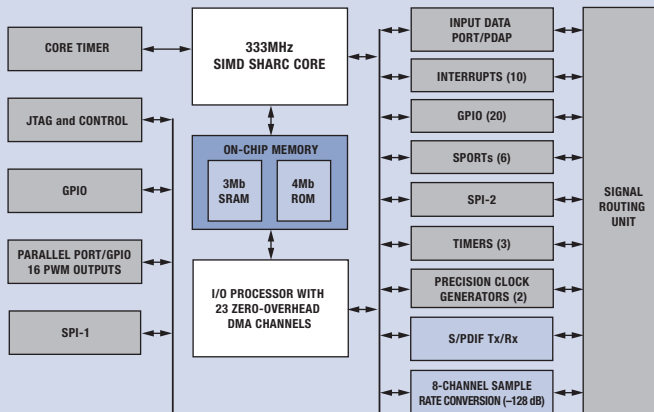
Features

- 333 MHz/2 GFLOPS SIMD SHARC core supporting IEEE 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 3 Mb SRAM; 4 Mb ROM embedded with the latest industry-standard audio decode and postprocessing algorithms
- 25 zero-overhead DMA channels
- Digital applications interface (DAI) enabling user-definable access to peripherals, including an S/PDIF Tx/Rx, 8-channel asynchronous sample rate converter, and Digital Transmission Content Protection hardware accelerator
- 6 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- 16 pulse-width modulation (PWM) channels
- 3 full-featured timers
- PLL capable of 1× to 32× frequency multiplication
- 16-bit parallel port
- Core voltage: 1.2 V

Applications

- Consumer home theater
- Digital audio amplifiers
- Professional audio

Part Number[1]	Max (MHz)	On-Chip Memory SRAM/ROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21366BBC-1AA	333	3/4	−40 to +85	3 timers, 6 SPORTs, DAI, 2 SPIs, 2 PCGs, PWM, 8-channel ASRC, S/PDIF Rx/Tx, integrated audio decoders in ROM	136-ball CSP_BGA	Contact ADI
ADSP-21366BBCZ-1AA	333	3/4	−40 to +85		136-ball CSP_BGA	
ADSP-21366BSWZ-1AA	333	3/4	−40 to +85		144-lead LQFP E-Pad	
ADSP-21366KBC-1AA	333	3/4	0 to 70		136-ball CSP_BGA	
ADSP-21366KBCZ-1AA	333	3/4	0 to 70		136-ball CSP_BGA	
ADSP-21366KSWZ-1AA	333	3/4	0 to 70		144-lead LQFP E-Pad	
ADSP-21366YSWZ-2AA	200	3/4	−40 to +105		144-lead LQFP E-Pad	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

License agreement required from IP holders before purchase of the ADSP-21366.

ADSP-21363/ADSP-21364 SHARC Processors
333 MHz Performance for Broad Market Applications

The ADSP-21363/ADSP-21364 provide superior performance—333 MHz/ 2 GFLOPS—within the third generation SHARC processor family. This level of performance makes the ADSP-21363/ADSP-21364 particularly well-suited to address the increasing requirements of a broad range of applications. High core performance, combined with audiocentric peripherals, including a high precision, 8-channel asynchronous sample rate converter and 16-bit parallel port, makes the ADSP-21363/ADSP-21364 an excellent choice.

ADSP-21363/ADSP-21364 Block Diagram
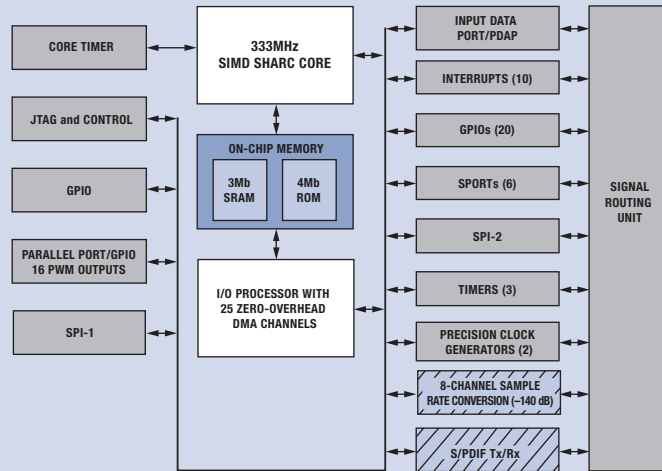
140dB SRC AVAILABLE FOR THE ADSP-21364 ONLY. S/PDIF AND SRC NOT AVAILABLE ON THE ADSP-21363.

Features

- 333 MHz/2 GFLOPS SIMD SHARC core supporting IEEE 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 3 Mb SRAM, 4 Mb ROM
- 25 zero-overhead DMA channels
- High precision, 8-channel asynchronous sample rate converter based on the award-winning AD1896
- Digital applications interface (DAI) enabling user-definable access to peripherals, including an input data port (IDP) and general-purpose I/O
- 6 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- 16 pulse-width modulation (PWM) channels
- 3 full-featured timers
- PLL capable of 1× to 32× frequency multiplication
- 16-bit parallel port
- Core voltage: 1.2 V

Applications

- Automotive audio
- Consumer home theater
- Digital audio amplifiers
- Professional audio

Part Number[1]	Max (MHz)	On-Chip Memory SRAM/ROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21363BBC-1AA	333	3/4	−40 to +85	3 timers, 6 SPORTs, 2 SPIs, S/PDIF Rx/Tx (not available on ADSP-21363), 8-channel ASRC (not available on ADSP-21363), 2 PCGs, PWM, DAI	136-ball CSP_BGA	20.22 to 29.13
ADSP-21363BBCZ-1AA	333	3/4	−40 to +85		136-ball CSP_BGA	
ADSP-21363BSWZ-1AA	333	3/4	−40 to +85		144-lead LQFP E-Pad	
ADSP-21363KBC-1AA	333	3/4	0 to 70		136-ball CSP_BGA	
ADSP-21363KBCZ-1AA	333	3/4	0 to 70		136-ball CSP_BGA	
ADSP-21363KSWZ-1AA	333	3/4	0 to 70		144-lead LQFP E-Pad	
ADSP-21363YSWZ-2AA	200	3/4	−40 to +105		144-lead LQFP E-Pad	
ADSP-21364BBC-1AA	333	3/4	−40 to +85		136-ball CSP_BGA	29.75 to 42.85
ADSP-21364BBCZ-1AA	333	3/4	−40 to +85		136-ball CSP_BGA	
ADSP-21364BSWZ-1AA	333	3/4	−40 to +85		144-lead LQFP E-Pad	
ADSP-21364KBC-1AA	333	3/4	0 to 70		136-ball CSP_BGA	
ADSP-21364KBCZ-1AA	333	3/4	0 to 70		136-ball CSP_BGA	
ADSP-21364KSWZ-1AA	333	3/4	0 to 70		144-lead LQFP E-Pad	
ADSP-21364YSWZ-2AA	200	3/4	−40 to +105		144-lead LQFP E-Pad	

NOTES

[1]Certain models available in automotive grade.

[2]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-21266 SHARC Processor
32-Bit Floating-Point Processor for Home Theater

The ADSP-21266 is a third generation SHARC processor optimized for consumer audio applications. This processor offers the same features as the ADSP-21262, with the addition of factory programmed ROM to contain the latest multichannel audio decoders from Dolby and DTS.

The ADSP-21266 is code-compatible with all prior SHARC processors and pin-compatible with third generation processors. The ADSP-21266 is based on a SIMD core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats, making them particularly suitable for high performance consumer audio applications, such as home theater systems and A/V receiver systems.

SHARC Melody Platform

The SHARC Melody platform combines high performance processors with optimized software, offering complete audio solutions to home theater manufacturers.

The ADSP-21266 is a large memory, high performance device targeted primarily at mid- to high-end home theater systems. SHARC Melody solutions are offered through on-chip ROM containing industry-standard audio decoder algorithms such as:

- PCM
- Dolby Digital
- Dolby Digital EX2
- Dolby Pro Logic® IIx
- DTS 5.1
- DTS ES®
- DTS Neo:6™ (cinema and music)
- DTS 96/24
- MPEG-2 AAC LC
- MPEG-2 (BC) 2 channel
- WMA Pro v7.1

Features

- 200 MHz (5 ns) SIMD SHARC core, capable of 1.2 GFLOPS
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 2 Mb SRAM; 4 Mb ROM embedded with industry-standard audio decode and postprocessing algorithms
- 16-bit parallel port
- 22 zero-overhead DMA channels
- Digital applications interface (DAI) enables user-definable access to peripherals, including precision clock generators, IDP, and general-purpose I/O
- 6 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- SPI-compatible, port-supporting master and slave modes
- 3 full-featured timers
- Software PLL capable of a variety of multiplier ratios
- 136-ball CSP_BGA (12 mm × 12 mm) and 144-lead LQFP (20 mm × 20 mm) packages
- Industrial grade BGA available
- Core voltage: 1.2 V

Applications

- Consumer home theater
- Professional audio
- Automotive audio

Part Number	Max (MHz)	On-Chip Memory SRAM/SROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21266SKBCZ-2B	200	2/4	0 to 70		136-ball CSP_BGA	
ADSP-21266SKBCZ-2C	200	2/4	0 to 70		136-ball CSP_BGA	
ADSP-21266SKBCZ-2D	200	2/4	0 to 70	3 timers, 6 SPORTs, 1 SPI, integrated audio decoders in ROM, 2 PCGs, DAI	136-ball CSP_BGA	Contact ADI
ADSP-21266SKSTZ-1B	150	2/4	0 to 70		144-lead LQFP	
ADSP-21266SKSTZ-1C	150	2/4	0 to 70		144-lead LQFP	
ADSP-21266SKSTZ-1D	150	2/4	0 to 70		144-lead LQFP	
ADSP-21266SKSTZ-2B	200	2/4	0 to 70		144-lead LQFP	
ADSP-21266SKSTZ-2C	200	2/4	0 to 70		144-lead LQFP	
ADSP-21266SKSTZ-2D	200	2/4	0 to 70		144-lead LQFP	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.
Z = RoHS compliant part.
License agreement required from IP holders before purchase of the ADSP-21266.

ADSP-21262 SHARC Processor
200 MHz, Low Cost, 32-/40-Bit Floating-Point Processor

The ADSP-21262 is a third generation SHARC programmable digital signal processor operating at up to 200 MHz. The design of the ADSP-21262 is based on a SIMD architecture that efficiently supports execution of 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats.

With its SIMD core operating at 200 MHz (a 5 ns instruction cycle time), the processor actually operates at up to 400 MMACS/1200 MFLOPS. With such a high bandwidth core, the ADSP-21262 is capable of executing 1024-point complex FFT operations in just 46 μs. This is more than 2.6 times faster than comparatively priced processors and provides optimal performance in audio as well as in broad market processor applications.

Digital Applications Interface (DAI) for Simplified I/O System Development

The ADSP-21262 introduces the DAI, an architecture that enables complete software programmability of various peripherals. The flexibility and ease of use of the SHARC programming model, combined with the DAI, allow manufacturers to deploy one hardware configuration into multiple product offerings with different I/O requirements.

Features

- 200 MHz (5 ns) SIMD SHARC core, capable of 1.2 GFLOPS
- Code-compatible with all SHARC processors
- Pin-compatible with all SHARC ADSP-2126x and ADSP-2136x processors
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 2 Mb on-chip, dual-ported SRAM
- 2.4 GBps on-chip bandwidth
- 22 zero-overhead DMA channels
- 6 independent serial ports—supports standard DSP serial, I²S, left justified sample pair, and TDM modes
- SPI-compatible interface and a 16-bit parallel port
- Digital applications interface (DAI)
- 4 timers: 1 core and 3 general-purpose
- 136-ball CSP_BGA (12 mm ×12 mm) and 144-lead LQFP (20 mm × 20 mm) packages available in commercial and industrial temperature ranges
- Core voltage: 1.2 V

Applications

- Professional audio
- Consumer A/V receivers
- Automotive audio
- Medical appliances
- Voice recognition
- Test and measurement equipment
- Telephony
- Wireless communications

ADSP-21262 Block Diagram
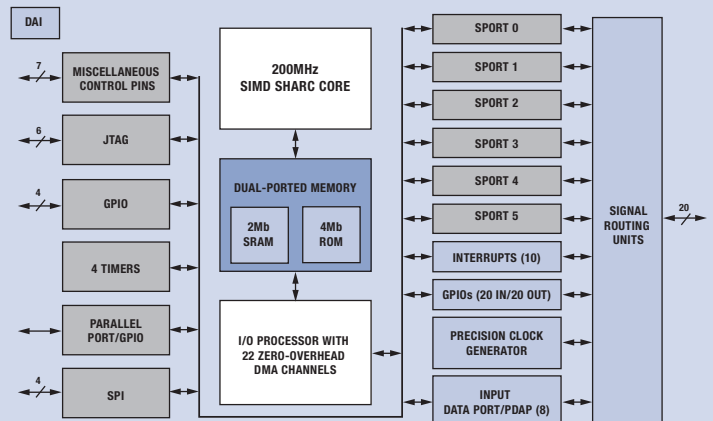
Part Number[1]	Max (MHz)	On-Chip Memory SRAM/SROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21262SBBC-150	150	2/4	−40 to +85		136-ball CSP_BGA	
ADSP-21262SBBCZ150	150	2/4	−40 to +85		136-ball CSP_BGA	
ADSP-21262SKBC-200	200	2/4	0 to 70	3 timers, 6 SPORTs, 1 SPI, 2 PCGs, DAI	136-ball CSP_BGA	17.15 to 25.35
ADSP-21262SKBCZ200	200	2/4	0 to 70		136-ball CSP_BGA	
ADSP-21262SKSTZ200	200	2/4	0 to 70		144-lead LQFP	

NOTES
[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-21261 SHARC Processor
150 MHz, Low Cost, 32-Bit Floating-Point Processor

The ADSP-21261 is the lowest cost member of the third generation of SHARC programmable digital signal processors. It is based on the SIMD SHARC core that supports execution of 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats.

With its core running at 150 MHz (6.67 ns instruction cycle time), the ADSP-21261 is capable of executing 1024-point complex FFT operations in 61 μs. The processor's single-instruction, multiple-data (SIMD) mode effectively doubles the processor performance.

The ADSP-21261 is designed with a high level of functional integration, including 1 Mb of on-chip, dual-ported SRAM, which enables sustained processor and I/O performance without the need for external memory. System I/O is achieved through four full-duplex serial ports, four timers, a 16-bit parallel port, a serial peripheral interface (SPI), 18 zero-overhead direct memory access (DMA) channels delivering fast data transfers without processor intervention, and an innovative digital applications interface (DAI), which provides the user complete software control through its signal routing unit (SRU).

Features

- 150 MHz (6.67 ns) SIMD SHARC core, capable of 900 MFLOPS peak performance
- Code-compatible with all SHARC processors
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 1 Mb on-chip, dual-ported SRAM
- 18 zero-overhead DMA channels
- 4 independent serial ports that support standard DSP serial mode, I²S mode, left justified sample-pair mode, and TDM mode
- SPI-compatible interface and a 16-bit parallel port
- Digital applications interface (DAI)
- Software configurable PLL providing many possible multiplier ratios
- 4 timers: 1 core and 3 general-purpose
- 136-ball CSP_BGA (12 mm × 12 mm) and 144-lead LQFP (20 mm × 20 mm) packages available in commercial temperature range
- Core voltage: 1.2 V

Applications

- Medical appliances
- Test and measurement equipment
- Voice recognition
- Professional audio
- Consumer A/V receivers
- Automotive audio
- Telephony
- Wireless communications

ADSP-21261 Block Diagram
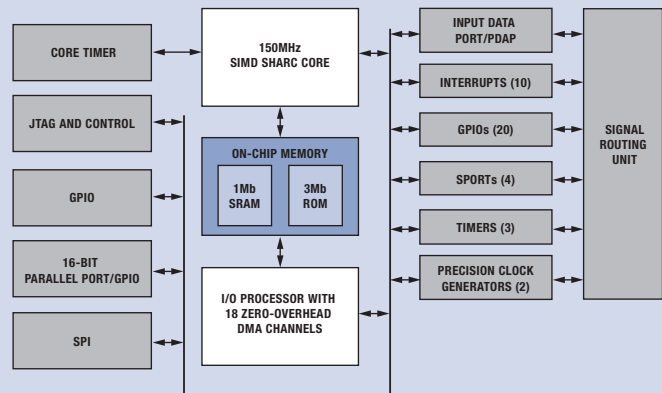
Part Number	Max (MHz)	On-Chip Memory SRAM/SROM (Mb)	Ambient Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21261SKBC-150	150	1/3	0 to 70	3 timers, 4 SPORTs, 1 SPI, 2 PCGs, DAI, 2 link ports, DMA controller	136-ball CSP_BGA	6.64 to 7.68
ADSP-21261SKBCZ150	150	1/3	0 to 70		136-ball CSP_BGA	
ADSP-21261SKSTZ150	150	1/3	0 to 70		144-lead LQFP	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.
Z = RoHS compliant part.

ADSP-21161N SHARC Processor
100 MHz, Low Cost, 32-Bit Processor

The 32-bit floating-point programmable ADSP-21161N processor is based on a SIMD SHARC architecture and is optimized for single processor and small multiprocessor systems.

The ADSP-21161N core operates at up to 100 MHz and is capable of 600 MFLOPS. The core is supported by 12 GPIO flags, SPI ports, and serial ports, and it supports external SDRAM and SBSRAM, which make the ADSP-21161N an excellent choice for audio and broad market multiprocessing applications.

Benefits

- Cluster multiprocessing and two 100 MBps link ports simplify connection and communication for multiprocessing
- SDRAM controller improves large DRAM bank throughput
- 4 serial ports allow 16 channels of data to be transferred in/out of the processor

Features

- 100 MHz (10 ns) SIMD SHARC processor core
- 600 MFLOPS (32-bit floating-point data), 600 MOPS (32-bit fixed-point data)
- Code-compatible with ADSP-21x6x SHARC processors
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point math
- Single-cycle instruction execution, including SIMD operations in both computational units
- 1 Mb on-chip, dual-ported SRAM
- 2.4 GBps on-chip data bandwidth
- 14 zero-overhead DMA channels
- 4 synchronous serial ports with I²S support
- Serial ports support 128-channel TDM frames with selection of companding on a per channel basis
- Integrated support for SDRAM and SBSRAM external memories
- Support for single-cycle, 100 MHz instruction execution from 48-bit wide external memories
- Core voltage: 1.8 V

Applications

- Speech recognition
- Professional and high end consumer audio
- Automotive entertainment
- Fingerprint recognition
- Digital audio broadcast
- Wireless communications
- Motor control
- Global positioning systems
- Medical equipment
- Telephony
- Test equipment

ADSP-21161N Block Diagram
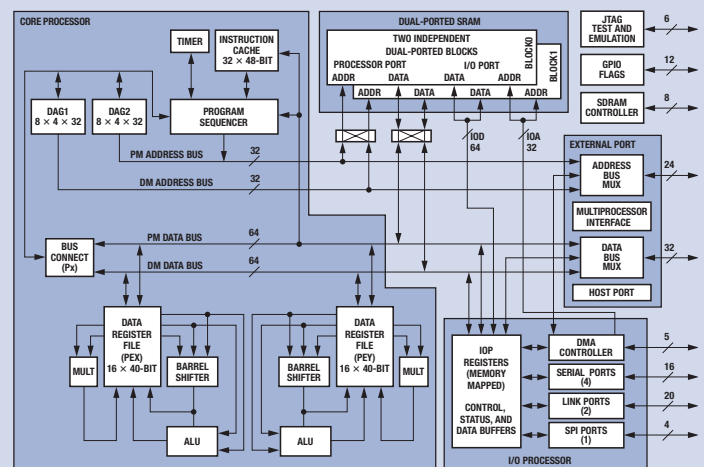
Part Number[1]	Max (MHz)	On-Chip Memory SRAM (Mb)	Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21161NCCA-100	100	1	−40 to +85 ambient	3 timers, 4 SPORTs, 1 SPI, 2 PCGs, DAI, 2 link ports, DMA controller	225-ball CSP_BGA	26.17 to 36.27
ADSP-21161NCCAZ100	100	1	−40 to +85 ambient		225-ball CSP_BGA	
ADSP-21161NKCA-100	100	1	0 to 85 case		225-ball CSP_BGA	
ADSP-21161NKCAZ100	100	1	0 to 85 case		225-ball CSP_BGA	

NOTES

[1] Certain models available in automotive grade.

[2] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-21160 SHARC Processor
100 MHz, 32-Bit Processor for Multiprocessing Applications

The ADSP-21160 family introduces single-instruction, multiple-data (SIMD) processing to the SHARC processor family. While maintaining code compatibility with previous SHARC family members, the SIMD architecture provides up to a 2× increase in performance on a cycle-by-cycle basis. Like all SHARC processors, the ADSP-21160 offers native support of 32-bit fixed-point and 32-/40-bit floating-point data types.

Designed specifically for multiprocessing applications, the ADSP-21160 offers a balanced architecture with 600 MFLOPS core performance, 4 Mb on-chip SRAM, zero-overhead DMAs, large I/O bandwidth, and multiprocessing support through cluster and link port interfaces.

Applications

- Audio
- Medical
- Military
- 3D graphics
- Imaging
- Communications

Features

- Glueless clusters of up to 6 SHARC processors
- Link ports for 2D and 3D arrays
- Distributed bus arbitration
- Unified memory space
- Link ports provide up to 80 MBps I/O each
- 320 MBps external port
- Hardware support for semaphores
- 100 MHz (10.5 ns) core instruction rate
- Single-cycle instruction execution, including SIMD operations in both computational units
- 570 MFLOPS peak and 380 MFLOPS sustained performance (based on FIR)
- Dual data address generators (DAGs) with modulo and bit-reverse addressing
- 4 Mb dual-ported SRAM
- Zero-overhead looping and single-cycle loop setup, providing efficient program sequencing
- IEEE 1149.1 JTAG standard test access port and on-chip emulation
- Core voltage: 1.8 V to 2.5 V

ADSP-21160 Block Diagram
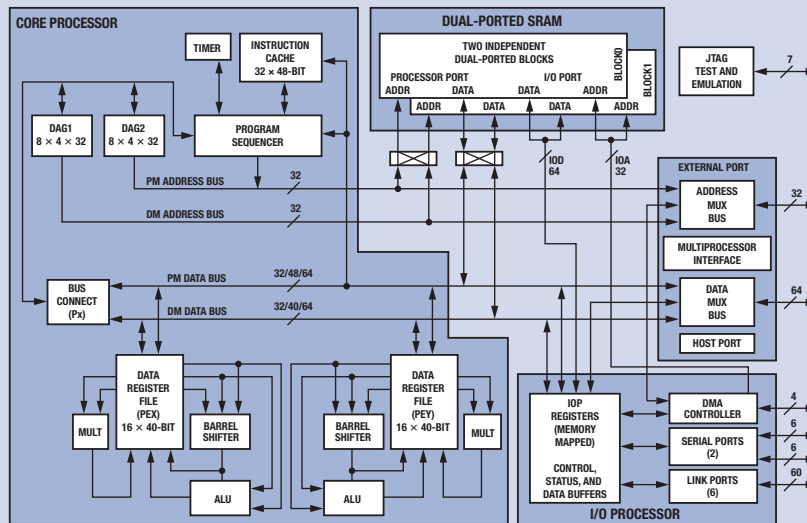
Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21160MKB-80	80	4	0 to 85 case		400-ball PBGA	
ADSP-21160MKBZ-80	80	4	0 to 85 case	2 SPORTs,	400-ball PBGA	
ADSP-21160NCB-100	100	4	−40 to +100 case	4 link ports,	400-ball PBGA	169.49 to 209.25
ADSP-21160NCBZ-100	100	4	−40 to +100 case	DMA controller	400-ball PBGA	
ADSP-21160NKB-100	100	4	0 to 85 case		400-ball PBGA	
ADSP-21160NKBZ-100	100	4	0 to 85 case		400-ball PBGA	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

Z = RoHS compliant part.

ADSP-21065L SHARC Processor
32-Bit Processor

The ADSP-21065L is a broad market, programmable 32-bit SHARC processor that allows users to program with equal efficiency in both fixed-point and floating-point arithmetic. This programming flexibility, combined with the high performance core and integrated peripherals, make the ADSP-21065L an outstanding price/performance value for a broad base of consumer, communications, automotive, industrial, and computer applications.

The ADSP-21065L is code-compatible with the ADI SHARC processor family and, as such, customers have immediate access to software and hardware development tools from ADI and SHARC processor third parties.

Applications

- Keyless entry using voice analysis/recognition
- Barcode scanners
- Imaging
- Ultrasound equipment
- Digital oscilloscopes
- Fingerprint recognition
- Professional audio
- Automotive audio
- Consumer audio

Features

- 544 kb configurable, dual-ported, on-chip memory
- 64M × 32-bit word external address space
- 198 MFLOPS (32-bit floating-point)
- 198 MOPS (32-bit fixed-point)
- Glueless SDRAM interface
- 2 serial transmit/receive ports support 32-channel TDM
- I²S mode supports up to 16 channels
- 2 timers with event capture and PWM options
- 12 programmable I/O pins
- 10 DMA channels
- Glueless multiprocessing with two ADSP-21065L processors
- Code-compatible with all SHARC processors
- 208-lead MQFP, 196-ball CSP_BGA packages
- Core voltage: 3.3 V

ADSP-21065L Block Diagram
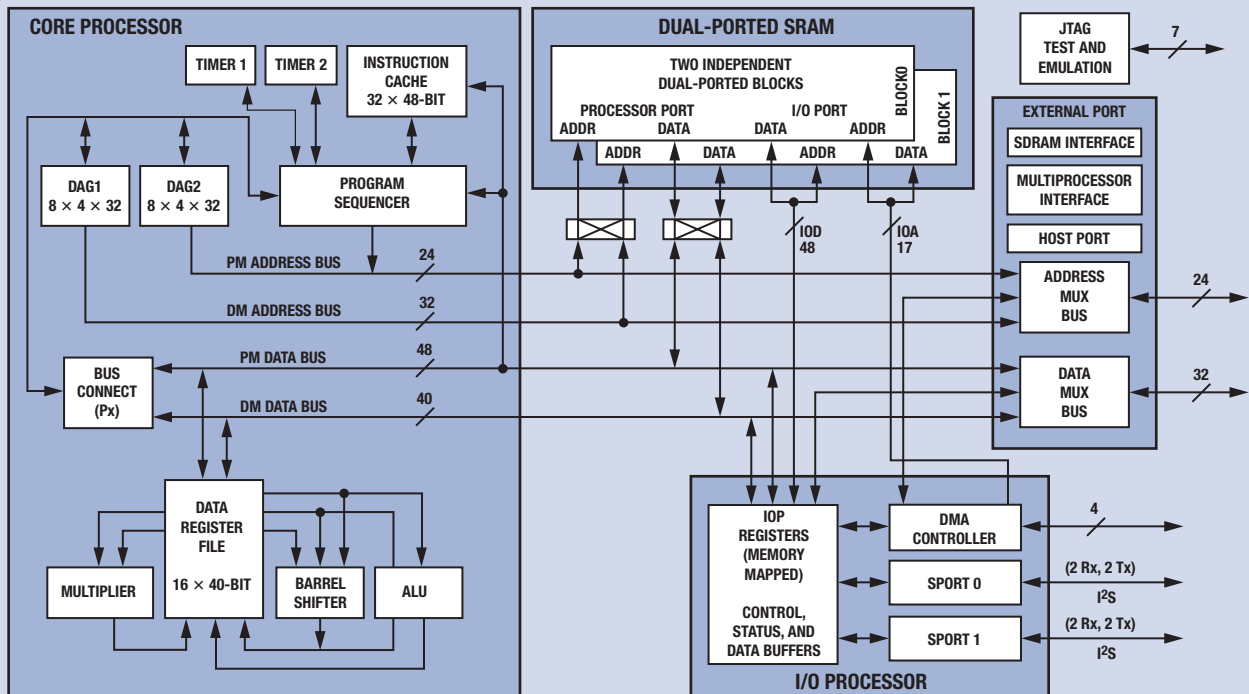
ADSP-21065L SHARC Processor
32-Bit Processor

Part Number	Max (MHz)	On-Chip Memory SRAM (kb)	Temperature Range (°C)	Key Peripherals	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21065LCCA-240	60	544	−40 to +100 case		196-ball CSP_BGA	
ADSP-21065LCCAZ-240	60	544	−40 to +100 case		196-ball CSP_BGA	
ADSP-21065LCSZ-240	60	544	−40 to +100 case		208-lead MQFP	
ADSP-21065LKCA-240	60	544	0 to 85 case	2 SPORTs, DMA controller, 2 timers	196-ball CSP_BGA	22.85 to 69.93
ADSP-21065LKCA-264	66	544	0 to 85 case		196-ball CSP_BGA	
ADSP-21065LKCAZ240	60	544	0 to 85 case		196-ball CSP_BGA	
ADSP-21065LKCAZ264	66	544	0 to 85 case		196-ball CSP_BGA	
ADSP-21065LKSZ-240	60	544	0 to 85 case		208-lead MQFP	
ADSP-21065LKSZ-264	66	544	0 to 85 case		208-lead MQFP	

NOTES

[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

L = indicates 3.3 V operation.

Z = RoHS compliant part.

SigmaDSP Audio Processors

SigmaDSP digital audio processors enable anyone to use a fully programmable audio DSP that is easily configurable through the SigmaStudio Graphical Development Tool. The latest SigmaDSP products address the automotive and portable audio markets with our highest performance SigmaDSP and most power-conscious processor. The ADAU1442, ADAU1445, and ADAU1446 SigmaDSP devices combine a 172 MHz core with a routing matrix and asynchronous sample rate converters. The routing matrix allows connection of many digital sources running at different sample rates to seamlessly connect to the audio processor. The first low power SigmaDSP processors, the ADAU1761 and ADAU1781, include the same powerful SigmaDSP found in other parts and are paired with stereo ADCs and DACs at an SNR performance greater than 100 dB.

The first low power SigmaDSP devices, the ADAU1761 and ADAU1781, include the same powerful SigmaDSP found in other parts and is paired with stereo ADCs and DACs at an SNR performance greater than 100 dB.

The AD1940 and AD1941 feature high processing power with more I/O channels. The ADAU1701 and ADAU1702 incorporate full analog I/O, digital I/O, and standalone functionality to provide a full audio processing system on a single chip. The ADAU1401 has similar functionality to the ADAU1701, but is designed specifically for the automotive market and specified over the extended temperature range.

SigmaDSP Product Selection Tables

Part Number	Instructions/ Cycle	Data RAM (k Words)	Digital I/O	Analog I/O Channels	GPIOs	Other Features	Description	Package	Price @1k ($U.S.)
AD1940	1536	6	16/16	0/0	0		Multichannel 28-/56-bit audio processor with 4-wire SPI control interface.	48-lead LQFP	8.45
AD1941	1536	6	16/16	0/0	0		Multichannel 28-/56-bit audio processor with 2-wire I²C control interface	48-lead LQFP	8.45
ADAU1401A	1024	2	8/8	4/2	12		28-/56-bit automotive audio processor with 2 ADCs and 4 DACs	48-lead LQFP	5.68
ADAU1442	3584	8	24/24	0/0	12	8 × 2-channel ASRC, selfboot from EEPROM	Digital audio processor with flexible audio routing matrix, 2 × 8-channel ASRC	100-lead LQFP	9.96
ADAU1445	3584	8	24/24	0/0	12	2 × 8-channel ASRC, selfboot from EEPROM	Digital audio processor with flexible audio routing matrix, 8 × 2-channel ASRC	100-lead LQFP	9.31
ADAU1446	3584	8	24/24	0/0	12	Selfboot from EEPROM	Digital audio processor with flexible audio routing matrix	100-lead LQFP	8.28
ADAU1461	1024	4	8/8	2/2	4	Digital microphone inputs, headphone amplifier, fractional PLL	Stereo, automotive grade, 96 kHz, 24-bit audio codec with integrated PLL	32-lead LFCSP	4.89
ADAU1701	1024	2	8/8	4/2	12	Selfboot from EEPROM	28-/56-bit audio processor with 2 ADCs and 4 DACs	48-lead LQFP	4.52
ADAU1702	512	0.5	8/8	4/2	12	Selfboot from EEPROM	28-/56-bit audio processor with 2 ADCs and 4 DACs	48-lead LQFP	3.57
ADAU1761	1024	4	8/8	2/2	4	Digital microphone inputs, headphone amplifier, fractional PLL	Stereo, low power, 96 kHz, 24-bit audio codec with integrated PLL	32-lead LFCSP	3.91
ADAU1781		32-lead LFCSP	8/8	2/2	5	Digital microphone inputs, mono speaker amplifier, fractional PLL	SigmaDSP low-noise stereo audio codec for portable applications	32-lead LFCSP	3.19

AD1940/AD1941
SigmaDSP Multichannel 28-Bit Audio Processor

The AD1940/AD1941 are complete 28-bit, single-chip, multichannel audio DSPs, for equalization, multiband dynamics processing, delay compensation, speaker compensation, and image enhancement. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of perceived audio quality.

The signal processing used in the AD1940/AD1941 is comparable to that found in high end studio equipment. Most of the processing is done in full, 56-bit double-precision mode, resulting in very good low level signal performance and the absence of limit cycles or idle tones. The dynamics processor uses a sophisticated, multiple breakpoint algorithm often found in high end broadcast compressors.

The AD1940/AD1941 are fully programmable DSPs. Easy to use software allows the user to graphically configure a custom signal processing flow using blocks such as biquad filters, dynamics processors, and surround sound processors. An extensive control port allows click-free parameter updates, along with readback capability from any point in the algorithm flow.

The AD1940's digital input and output ports allow a glueless connection to ADCs and DACs by multiple, 2-channel serial data streams or TDM data streams. When in TDM mode, the AD1940 can input eight or 16 channels of serial data, and can output either eight or 16 channels of serial data. The input and output port configurations can be individually set. The AD1940 is controlled via a 4-wire SPI port, while the AD1941 is controlled with an I²C port.

Applications
- Automotive sound systems
- Digital televisions
- Home theater systems (Dolby Digital/DTS postprocessor)
- Multichannel audio systems
- Mini-component stereos
- Multimedia audio
- Digital speaker crossover
- Musical instruments
- In-seat sound systems (aircrafts/motor coaches)

Features
- 16-channel digital audio processor
- Accepts sample rates up to 192 kHz
- 28-bit $\times$ 28-bit multiplier with full 56-bit accumulator
- Fully programmable program RAM for custom program download
- Parameter RAM allows complete control of 1024 parameters
- SPI (AD1940) or I²C (AD1941) control port features safeload for transparent parameter updates and complete mode and memory transfer control
- Hardware-accelerated DSP core

AD1940/AD1941 Block Diagram
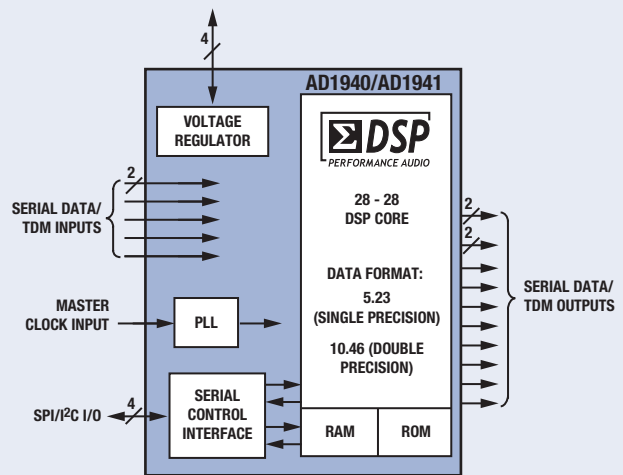
ADAU1401A
SigmaDSP 28-/56-Bit Automotive Audio Processor with Two ADCs and Four DACs

The ADAU1401A is a complete, single-chip audio system with 28-/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal processing includes equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. This processing can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, providing dramatic improvements in perceived audio quality.

The signal processing of the ADAU1401A is comparable to that found in high end studio equipment. Most processing is done in full 56-bit, double-precision mode, resulting in very good low level signal performance. The ADAU1401A is a fully programmable DSP. The easy to use SigmaStudio software allows the user to graphically configure a custom signal processing flow using blocks such as biquad filters, dynamics processors, level controls, and GPIO interface controls.

The ADAU1401A programs can be loaded on power-up either from a serial EEPROM through its own self-boot mechanism or from an external microcontroller. On power-down, the current state of the parameters can be written back to the EEPROM from the ADAU1401A to be recalled the next time the program is run.

Two Σ-Δ ADCs and four Σ-Δ DACs provide a 98.5 dB analog input to analog output dynamic. Each ADC has a THD + N of −83 dB and each DAC has a THD + N of −90 dB. Digital input and output ports allow a glueless connection to additional ADCs and DACs. The ADAU1401A communicates through an I²C bus or a 4-wire SPI port.

Applications

- Multimedia speaker systems
- MP3 player speaker docks
- Automotive head units
- Minicomponent stereos
- Digital televisions
- Studio monitors
- Speaker crossovers
- Musical instrument effects processors
- In-seat sound systems (aircraft/motor coaches)

Features

- 28-/56-bit, 50 MIPS digital audio processor
- 2 ADCs: SNR of 100 dB, THD + N of −83 dB
- 4 DACs: SNR of 104 dB, THD + N of −90 dB
- Complete standalone operation
- Self-boot from serial EEPROM
- Auxiliary ADC with 4-input mux for analog control
- GPIOs for digital controls and outputs
- Fully programmable with SigmaStudio graphical tool
- 28-bit × 28-bit multiplier with 56-bit accumulator for full double-precision processing
- Clock oscillator for generating master clock from crystal
- PLL for generating master clock from $64 \times f_s$, $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$ clocks
- Flexible serial data input/output ports with I²S-compatible, left-justified, right-justified, and TDM modes
- Sampling rates of up to 192 kHz supported
- On-chip voltage regulator for compatibility with 3.3 V systems
- 48-lead plastic LQFP

ADAU1401A Block Diagram
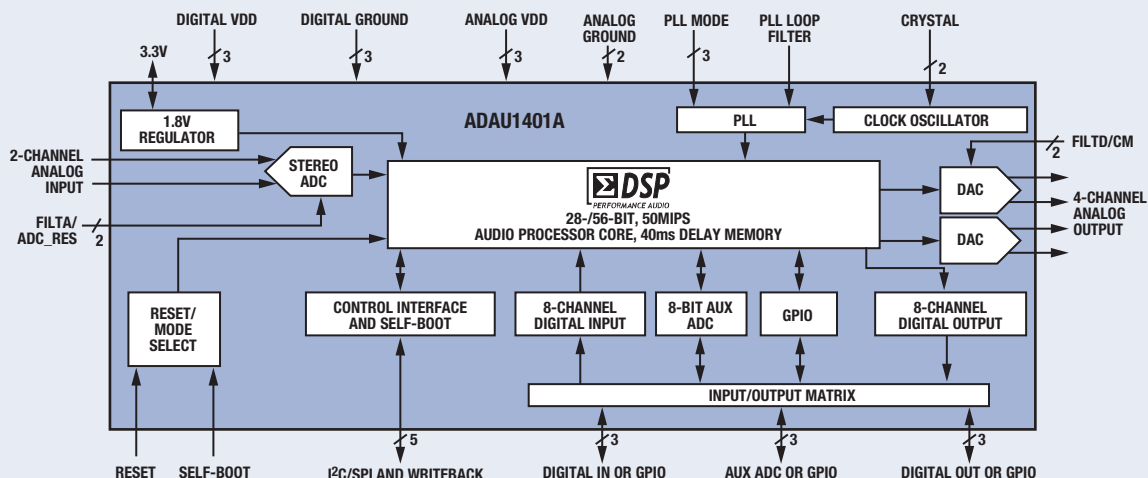
ADAU1442/ADAU1445/ADAU1446
SigmaDSP Digital Audio Processor with Flexible Audio Routing Matrix

The ADAU1442/ADAU1445/ADAU1446 are enhanced audio processors that allow full flexibility in routing all input and output signals. The SigmaDSP core features full 28-bit processing (56-bit in double-precision mode), synchronous parameter loading for ensuring filter stability, and 100% code efficiency with the SigmaStudio tools. This DSP allows system designers to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression, limiting, and third-party branded algorithms.

The flexible audio routing matrix (FARM) allows the user to multiplex inputs from multiple sources running at various sample rates to or from the SigmaDSP core. This drastically reduces the complexity of signal routing and clocking issues in the audio system. FARM includes up to eight stereo asynchronous sample rate converters (depending on the device model), Sony/Philips digital interconnect format (S/PDIF) input and output, and serial (I²S) and time division multiplexing (TDM) I/Os. Any of these inputs can be routed to the SigmaDSP core or to any of the asynchronous sample rate converters (ASRCs). Similarly, any one of the output signals can be taken from the SigmaDSP core or from any of the ASRC outputs. This routing scheme, which can be modified at any time via control registers, allows for maximum system flexibility.

The ADAU1442, ADAU1445, and ADAU1446 differ only in ASRC functionality and packaging. The ADAU1442/ADAU1445 contain 16 channels of ASRCs and are packaged in TQFP packages, whereas the ADAU1446 contains no ASRCs and is packaged in an LQFP. The ADAU1442 can handle nine clock domains, the ADAU1445 can handle three clock domains, and the ADAU1446 can handle one clock domain.

The ADAU1442/ADAU1445/ADAU1446 can be controlled in one of two operational modes: the settings of the chip can be loaded and dynamically updated through the SPI/I²C port, or the DSP can self-boot from an external EEPROM in a system with no microcontroller. There is also a bank of multipurpose (MP) pins that can be used as general-purpose digital I/Os or as inputs to the 4-channel auxiliary control ADC.

The ADAU1442/ADAU1445/ADAU1446 are supported by the SigmaStudio graphical development environment. This software includes audio processing blocks such as FIR and IIR filters, dynamics processors, mixers, low level DSP functions, and third-party algorithms for fast development of custom signal flows.

Applications

- Automotive audio processing
- Head units
- Navigation systems
- Rear-seat entertainment systems
- DSP amplifiers (sound system amplifiers)

Features

- Fully programmable audio digital signal processor (DSP) for enhanced sound processing
- Features SigmaStudio, a proprietary graphical programming tool for the development of custom signal flows
- 172 MHz SigmaDSP core; 3584 instructions per sample at 48 kHz
- 4k parameter RAM, 8k data RAM
- Flexible audio routing matrix (FARM)
- 24-channel digital input and output
- Up to 8 stereo asynchronous sample rate converters (from 1:8 up to 7.75:1 ratio and 139 dB DNR)
- Stereo S/PDIF input and output
- Supports serial and TDM I/O, up to f_s = 192 kHz
- Multichannel byte-addressable TDM serial port
- Pool of 170 ms digital audio delay (at 48 kHz)
- Clock oscillator for generating master clock from crystal
- PLL for generating core clock from common audio clocks
- I²C and SPI control interfaces
- Standalone operation
- Self-boot from serial EEPROM
- 4-channel, 10-bit auxiliary control ADC
- Multipurpose pins for digital controls and outputs
- Easy implementation of available third-party algorithms
- On-chip regulator for generating 1.8 V from 3.3 V supply
- 100-lead TQFP and LQFP packages
- Temperature range: −40°C to +105°C

ADAU1442/ADAU1445/ADAU1446

SigmaDSP Digital Audio Processor with Flexible Audio Routing Matrix

ADAU1442/ADAU1445/ADAU1446 Block Diagram
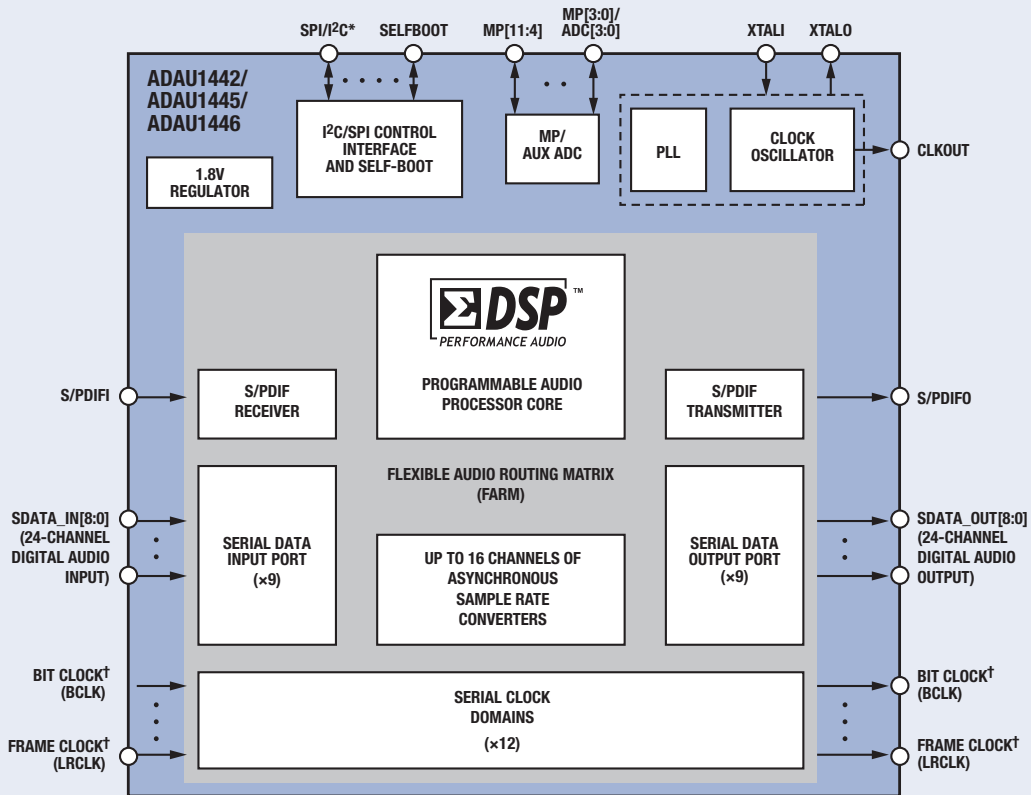
*SPI/I²C = THE ADDR0, CLATCH, SCL/CCLK, SDA/COUT, AND ADDR1/CDATA PINS.
†THERE ARE 12-BIT CLOCKS (BCLK[11:0]) AND 12 FRAME CLOCKS (LRCLK[11:0]) IN TOTAL. OF THE 12 CLOCKS, SIX ARE ASSIGNABLE, THREE MUST BE OUTPUTS, AND THREE MUST BE INPUTS.

ADAU1461
SigmaDSP Stereo, Low Power, 96 kHz, 24-Bit Audio Codec with Integrated PLL for Automotive Applications

The ADAU1461 is a low power, stereo audio codec with integrated digital audio processing that supports stereo 48 kHz record and playback at 35 mW from a 3.3 V analog supply. The stereo audio ADCs and DACs support sample rates from 8 kHz to 96 kHz as well as a digital volume control.

The SigmaDSP core features 28-bit processing (56-bit double precision). The processor allows system designers to compensate for the real-world limitations of microphones, speakers, amplifiers, and listening environments, resulting in a dramatic improvement in the perceived audio quality through equalization, multiband compression, limiting, and third-party branded algorithms.

The SigmaStudio graphical development tool is used to program the ADAU1461. This software includes audio processing blocks such as filters, dynamics processors, mixers, and low level DSP functions for fast development of custom signal flows.

The record path includes an integrated microphone bias circuit and six inputs. The inputs can be mixed and muxed before the ADC, or they can be configured to bypass the ADC. The ADAU1461 includes a stereo digital microphone input.

The ADAU1461 includes five high power output drivers (two differential and three single-ended), supporting stereo headphones, an earpiece, or other output transducer. AC-coupled or capless configurations are supported. Individual fine level controls are supported on all analog outputs. The output mixer stage allows for flexible routing of audio.

Applications

- Automotive head units
- Automotive amplifiers
- Navigation systems
- Rear-seat entertainment systems

Features

- SigmaDSP 28-/56-bit, 50 MIPS digital audio processor
- Fully programmable with SigmaStudio graphical tool
- 24-bit stereo audio ADC and DAC: >98 dB SNR
- Sampling rates from 8 kHz to 96 kHz
- Low power: 17 mW record, 18 mW playback, 48 kHz
- 6 analog input pins, configurable for single-ended or differential inputs
- Flexible analog input/output mixers
- Stereo digital microphone input
- Analog outputs: 2 differential stereo, 2 single-ended stereo, 1 mono headphone output driver
- PLL supporting input clocks from 8 MHz to 27 MHz
- Analog automatic level control (ALC)
- Microphone bias reference voltage
- Analog and digital I/O: 3.3 V
- I²C and SPI control interfaces
- Digital audio serial data I/O: stereo and time-division multiplexing (TDM) modes
- Software-controllable clickless mute
- GPIO pins for digital controls and outputs
- 32-lead, 5 mm × 5 mm LFCSP
- −40°C to +105°C operating temperature range
- Qualified for automotive applications

ADAU1461 Block Diagram
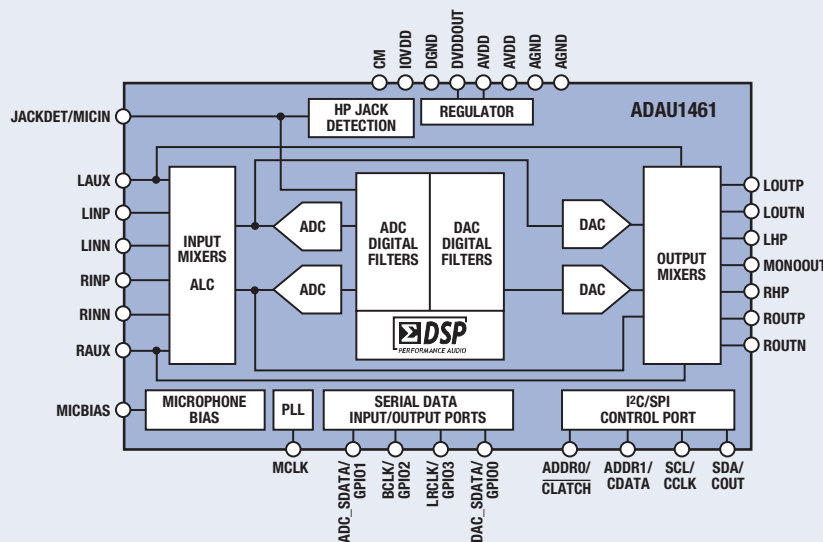
ADAU1701/ADAU1702
SigmaDSP 28-/56-Bit Audio Processor with Two ADCs and Four DACs

The ADAU1701/ADAU1702 are complete single-chip audio systems with a 28-/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal processing includes equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening and can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, providing dramatic improvements in perceived audio quality.

Its signal processing is comparable to that found in high end studio equipment. Most processing is done in full 56-bit, double-precision mode, resulting in very good low level signal performance. The ADAU1701 is a fully programmable DSP. The easy to use SigmaStudio software allows the user to graphically configure a custom signal processing flow using blocks such as biquad filters, dynamics processors, level controls, and GPIO interface controls.

ADAU1701/ADAU1702 programs can be loaded on power-up either from a serial EEPROM through its own self-boot mechanism or from an external microcontroller. On power-down, the current state of the parameters can be written back to the EEPROM from the ADAU1701 to be recalled the next time the program is run.

Two Σ-Δ ADCs and four Σ-Δ DACs provide a 98.5 dB analog input to analog output dynamic. Each ADC has a THD + N of −83 dB and each DAC has a THD + N of −90 dB. Digital input and output ports allow a glueless connection to additional ADCs and DACs. The ADAU1701/ADAU1702 communicates through an I²C bus or a 4-wire SPI port.

The ADAU1701 has 1024 instructions/cycle in the program RAM and 2k words of data memory, while the ADAU1702 has 512 instructions/cycle and 0.5k words of data memory.

Applications

- Multimedia speaker systems
- MP3 player speaker docks
- Automotive head units
- Minicomponent stereos
- Digital televisions
- Studio monitors
- Speaker crossovers
- Musical instrument effects processors
- In-seat sound systems (aircraft/motor coaches)

Features

- 28-/56-bit, 50 MIPS digital audio processor
- Two ADCs: SNR of 100 dB, THD + N of −83 dB
- Four DACs: SNR of 104 dB, THD + N of −90 dB
- Complete standalone operation
- Self-boot from serial EEPROM
- Auxiliary ADC with 4-input mux for analog control
- GPIOs for digital controls and outputs
- Fully programmable with SigmaStudio graphical tool
- 28-bit × 28-bit multiplier with 56-bit accumulator for full double-precision processing
- Clock oscillator for generating master clock from crystal
- PLL for generating master clock from $64 \times f_s$, $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$ clocks
- Flexible serial data input/output ports with I²S-compatible, left-justified, right-justified, and TDM modes
- Sampling rates up to 192 kHz supported
- On-chip voltage regulator for compatibility with 3.3 V systems
- 48-lead, plastic LQFP

ADAU1701/ADAU1702 Block Diagram
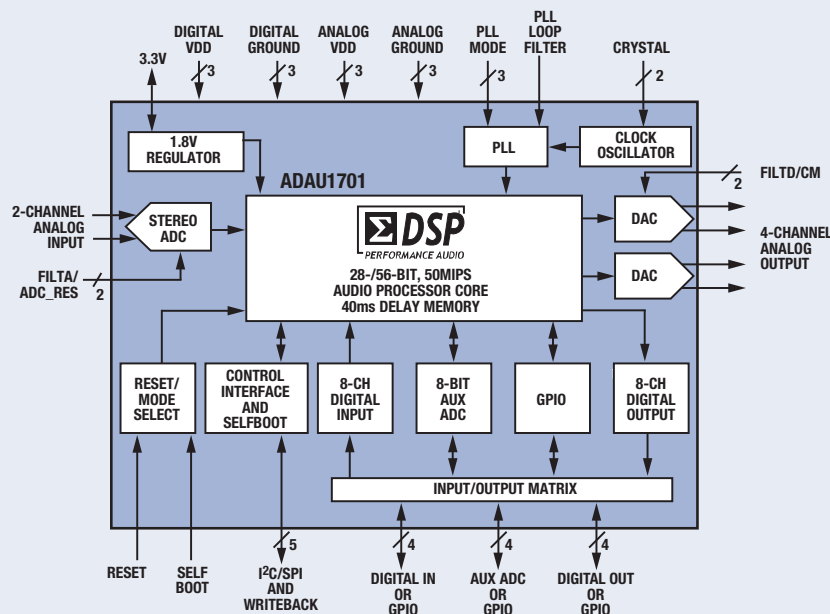
ADAU1761
SigmaDSP Stereo, Low Power, 96 kHz, 24-Bit Audio Codec with Integrated PLL

The ADAU1761 is a low power stereo audio codec with integrated digital audio processing that supports stereo 48 kHz record and playback at 14 mW from a 1.8 V analog supply. The stereo audio ADCs and DACs support sample rates from 8 kHz to 96 kHz as well as a digital volume control.

The SigmaDSP core features 28-bit processing (56-bit double precision). The processor allows system designers to compensate for the real-world limitations of microphones, speakers, amplifiers, and listening environments, resulting in a dramatic improvement in the perceived audio quality through equalization, multiband compression, limiting, and third-party branded algorithms.

The SigmaStudio graphical development tool is used to program the ADAU1761. This software includes audio processing blocks such as filters, dynamics processors, mixers, and low level DSP functions for fast development of custom signal flows.

The record path includes an integrated microphone bias circuit and six inputs. The inputs can be mixed and muxed before the ADC, or they can be configured to bypass the ADC. The ADAU1761 includes a stereo digital microphone input.

The ADAU1761 includes five high power output drivers (two differential and three single-ended), supporting stereo headphones, an earpiece, or other output transducer. AC-coupled or capless configurations are supported. Individual fine level controls are supported on all analog outputs. The output mixer stage allows for flexible routing of audio.
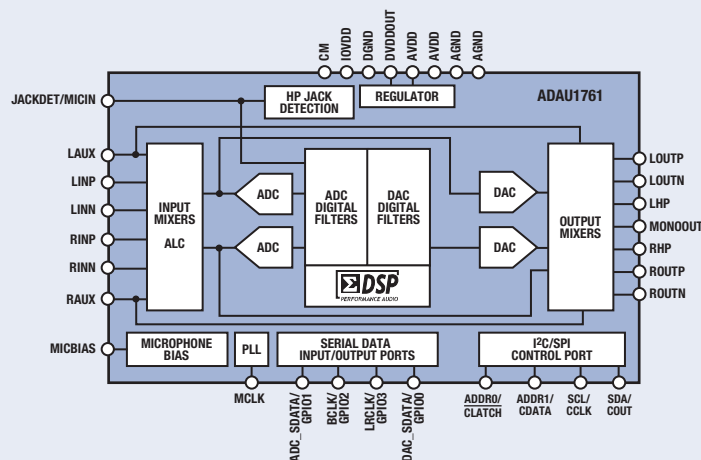
Applications

- Smartphones/multimedia phones
- Digital still cameras/digital video cameras
- Portable media players/portable audio players
- Phone accessories products

Features

- SigmaDSP 28-/56-bit, 50 MIPS digital audio processor
- Fully programmable with SigmaStudio graphical tool
- 24-bit stereo audio ADC and DAC: >98 dB SNR
- Sampling rates from 8 kHz to 96 kHz
- Low power: 7 mW record, 7 mW playback, 48 kHz at 1.8 V
- 6 analog input pins, configurable for single-ended or differential inputs
- Flexible analog input/output mixers
- Stereo digital microphone input
- Analog outputs: 2 differential stereo, 2 single-ended stereo, 1 mono headphone output driver
- PLL supporting input clocks from 8 MHz to 27 MHz
- Analog automatic level control (ALC)
- Microphone bias reference voltage
- Analog and digital I/O: 1.8 V to 3.65 V
- I²C and SPI control interfaces
- Digital audio serial data I/O: stereo and time-division multiplexing (TDM) modes
- Software-controllable clickless mute
- Software power-down
- GPIO pins for digital controls and outputs
- 32-lead, 5 mm × 5 mm LFCSP
- −40°C to +85°C operating temperature range

ADAU1761 Block Diagram

ADAU1781
SigmaDSP Low Noise Stereo Audio Codec for Portable Applications

The ADAU1781 is a low power, 24-bit stereo audio codec. The low noise DAC and ADC support sample rates from 8 kHz to 96 kHz. Low current draw and power saving modes make the ADAU1781 ideal for battery-powered audio applications.

A programmable SigmaDSP core provides enhanced record and playback processing to improve overall audio quality.

The record path includes two digital stereo microphone inputs and an analog stereo input path. The analog inputs can be configured for either a pseudo differential or a single-ended stereo source. A dedicated analog beep input signal can be mixed into any output path. The ADAU1781 includes a stereo line output and speaker driver, which makes the device capable of supporting dynamic speakers.

The serial control bus supports the I²C or SPI protocols, and the serial audio bus is programmable for I²S, left-justified, right-justified, or TDM mode. A programmable PLL supports flexible clock generation for all standard rates and available master clocks from 11 MHz to 20 MHz.

Applications
- Digital still cameras
- Digital video cameras

Features
- 24-bit stereo audio ADC and DAC
- 400 mW speaker amplifier (into 8 Ω load)
- Programmable SigmaDSP audio processing core
- Wind noise detection and filtering
- Enhanced stereo capture (ESC)
- Dynamics processing
- Equalization and filtering
- Volume control and mute
- Sampling rates from 8 kHz to 96 kHz
- Stereo pseudo differential microphone input
- Optional stereo digital microphone input pulse-density modulation (PDM)
- Stereo line output
- PLL supporting a range of input clock rates
- Analog and digital I/O 1.8 V to 3.3 V
- Software control via SigmaStudio graphical user interface
- Software-controllable, clickless mute
- Software register and hardware pin standby mode
- 32-lead, 5 mm × 5 mm LFCSP

ADAU1781 Block Diagram
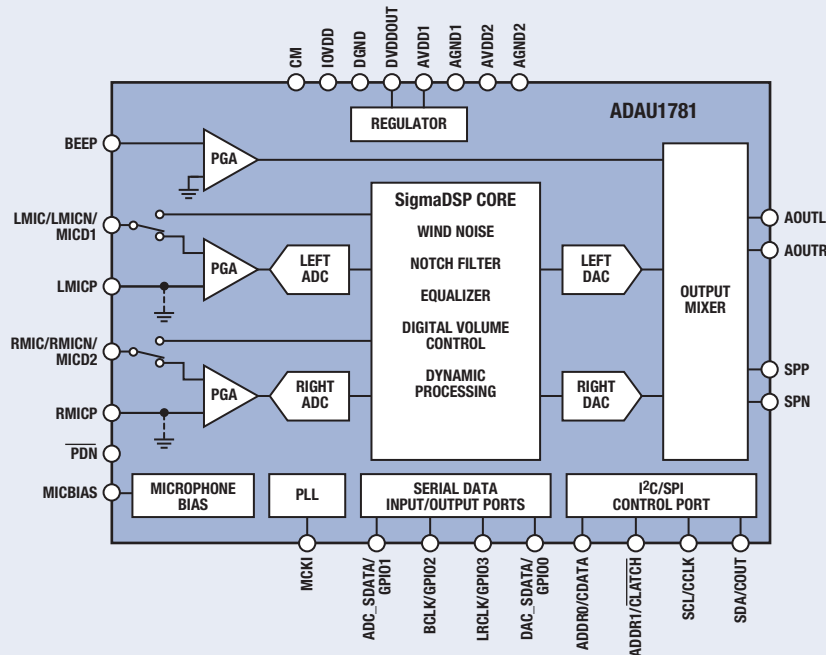
SigmaStudio
Graphical Development Tool for SigmaDSP

The SigmaStudio graphical development tool is the programming, development, and tuning software for the SigmaDSP audio processors. Familiar audio processing blocks can be wired together as in a schematic, and the compiler generates DSP-ready code and a control surface for setting and tuning parameters. This tool allows engineers with no DSP code writing experience to easily implement a DSP into their design and yet is still powerful enough to satisfy the demands of experienced DSP designers. SigmaStudio links with both Analog Devices evaluation boards and production designs to provide full in-circuit real-time IC control.

SigmaStudio includes an extensive library of algorithms to perform audio processing such as filtering, mixing, and dynamics processing, as well as basic low level DSP functions and control blocks. Advanced record-side processing algorithms such as enhanced stereo capture and wind noise detection are included in the standard libraries. Plug-in algorithms from Analog Devices and third-party partners can be added to SigmaStudio's drag-and-drop library.

Along with its graphical DSP signal flow development, SigmaStudio also includes other features to speed up the design cycle from product concept to release. SigmaStudio includes tools for intuitively setting control registers, calculating tables of filter coefficients, visualizing filter magnitude and phase responses, generating C header files, and sequencing a series of controls to ease your transition from SigmaStudio to system implementation on your microcontroller.

The latest version of SigmaStudio is available to download directly from the ADI website. The full set of signal processing libraries and features are included with the downloadable version.

Features

- Included algorithms
- IIR filters
- FIR filters
- Dynamics processors
- Volume controls
- Mixers, splitters
- Muxes, demuxes
- Sources
- GPIO conditioning
- Counters
- Basic DSP functions

SigmaDSP Audio Processors
SigmaDSP Evaulation Boards

Model	Description	Product / Alternate Product	Other ADI Components	Analog In / Analog Out	GPIO	Digital I/O / DC Supply	Price ($U.S.)
EVAL-AD1940AZ	Full-featured AD1940 SigmaDSP evaluation board with AD1939 and AD1974 codecs. It provides buffered analog inputs and ouputs as well as S/PDIF and digital I²S/TDM connectors. 6 V power supply and USBi are included in the package.	AD1940	AD1939, AD1974, AD8606, ADP3339	3 stereo TRS (3.5 mm)		USBi-I²C/SPI, S/PDIF I/O, I²S I/O (4/8, TDM)	699.00
		AD1941 (uses I²C instead of SPI)		4 stereo TRS (3.5 mm)		6 V	
EVAL-AD1940MINIBZ	Small AD1940 SigmaDSP evaluation board with AD1938 codec and buffered analog inputs and outputs. 6 V power supply and USBi are included in the package. This is the recommended evaluation board for the AD1940. The EVAL-AD1940AZ can be used if this board lacks some necessary functionality or interface.	AD1940	AD1938, ADP3336, ADM811, ADA4841	1 stereo TRS (3.5 mm)		USBi-I²C/SPI, I²S-I/O (1/3, TDM)	399.00
		AD1941 (uses I²C instead of SPI)		3 stereo TRS (3.5 mm)		6 V	
EVAL-ADAU1401EBZ	Full-featured ADAU1401 SigmaDSP evaluation board that operates all of the ADAU1401/ADAU1701/ADAU1702's functions with a full range of analog and digital inputs and outputs as well as a self-boot EEPROM. USBi, 6 V power supply, and an attachable GPIO control board are included in the package.	ADAU1401	AD8608, ADM811	1 stereo TRS (3.5 mm) or RCA	Rotary encoder, potentiometer, switches, push buttons, potentiometers, LEDs	USBi-I²C/SPI, S/PDIF I/O, I²S-I/O (TDM)	699.00
		ADAU1701 (not automotive qualified) ADAU1702 (not automotive qualified and has less memory)		2 stereo TRS (3.5 mm) or RCA		6 V	
EVAL-ADAU1701MINIZ	Small ADAU1701 SigmaDSP evaluation board with self-boot EEPROM and stereo 2 W Class-D amplifier. USBi is included in the package and it provides the 5 V power supply for the board. This is the recommended board for evaluation of the ADAU1701 and ADAU1702. The EVAL-ADAU1401EBZ can be used if this board lacks some necessary functionality or interface.	ADAU1701	SSM2306, ADM811, ADP3336	1 stereo TRS (3.5 mm)	3 LED, 3 push button, 1 potentiometer	USBi-I²C/SPI	195.00
		ADAU1401 (automotive qualified) ADAU1702 (has less memory)		Stereo speaker, 1 stereo TRS (3.5 mm)		5 V	
EVAL-ADAU1442EBZ	Full-featured ADAU1442 SigmaDSP evaluation board with a full set of analog and digital input/output connections, including I²S, TDM, and S/PDIF. USBi, 6 V power supply, and an attachable GPIO control board are included in the package.	ADAU1442	AD1938 (2), AD8608, ADP3336, ADP3339, ADM811	4 stereo TRS (3.5 mm)	Rotary encoder, potentiometer, switches, push buttons, potentiometers, LEDs	USBi-I²C/SPI, S/PDIF I/O, I²S-I/O (TDM)	699.00
		ADAU1445 (has less SRCs)		8 stereo TRS (3.5 mm)		6 V	
EVAL-ADAU1446EBZ	Full-featured ADAU1446 SigmaDSP evaluation board with a full set of analog and digital input/output connections, including I²S, TDM, and S/PDIF. USBi, 6 V power supply, and an attachable GPIO control board are included in the package.	ADAU1446	AD1938 (2), AD8608, ADP3336, ADP3339, ADM811	4 stereo TRS (3.5 mm)	Rotary encoder, potentiometer, switches, push buttons, potentiometers, LEDs	USBi-I²C/SPI, S/PDIF I/O, I²S-I/O (TDM)	699.00
				8 stereo TRS (3.5 mm)		6 V	
EVAL-ADAU1761Z	Full-featured ADAU1761 SigmaDSP evaluation board that operates most functions of the ADAU1761 with a full range of analog and digital inputs and outputs including the digital microphone and capless headphones. USBi is included in the package and it provides the 5 V power supply for the board.	ADAU1761	AD1938 (2), AD8608, ADP3336	2 differential TRS, 1 stereo TRS (3.5 mm)	Push buttons, LEDs, switches	USBi-I²C, I²S-I/O (1/1, TDM), stereo digital mic	195.00
		ADAU1461 (automotive qualified) ADAU1361 (has no SigmaDSP-emulation possible with ADAU1761)		2 differential and stereo TRS, 1 stereo headphone TRS (3.5 mm)		5 V	
EVAL-ADAU1781Z	Full-featured ADAU1781 SigmaDSP evaluation board that operates all functions of the ADAU1781 with a full range of analog and digital inputs and outputs including digital microphones and capless headphones. MEMS microphones and a speaker are included on the PCB. USBi is included in the package and it can provide the 5 V power supply for the board.	ADAU1781	ADMP401 (2), ADP1711, ADP3339, AD8397	2 differential TRS, 1 stereo TRS (3.5 mm), 1 mono beep TRS (3.5 mm), 2 ADMP401 omni MEMS microphones	Push buttons, LEDs	USBi-I²C/SPI, I²S-I/O (1/1, TDM), stereo digital mic	195.00
		ADAU1381/ADAU1382 (have no SigmaDSP-emulation possible with ADAU1761)		1 stereo headphone TRS (3.5 mm), mono speaker out, built-in mono speaker		5 V	
EVAL-ADUSB2EBZ "USBi"	USB to I²C/SPI interface board, also called USBi. This board connects to all SigmaDSP evaluation boards and provides the USB to I²C/SPI conversion. It is the interface between the SigmaDSP evaluation boards and the SigmaStudio software tools. USBi is included with all SigmaDSP evaluation boards but can also be ordered seperately. It ships with USB cable.					USB input, I²C/SPI output	95.00
						5 V (USB)	
SigmaStudio	The SigmaStudio tools package is ADI's award winning software for graphically programming SigmaDSP ICs and controlling evaluation boards. This software should be used with all SigmaDSP evaluation boards and is provided free of charge to evaluation board users.						Free

TigerSHARC Processor Family
Highest Performance Processor for Multiprocessor Systems

The TigerSHARC processor family offers the industry's highest performance per watt and per square inch of board space for the most demanding signal and image processing applications. Its patented link port technology allows glueless interprocessor communication within arrays of two or more TigerSHARC processors, delivering unbounded performance in terms of MMACS and MFLOPS.

Based on a 128-bit static superscalar architecture, TigerSHARC processors offer native support of fixed- and floating-point data types and a balanced combination of computational performance, I/O bandwidth, and memory integration. Together, this yields sustained DSP system-level performance that is two to four times greater than conventional DSPs or microprocessors with vector processing units.

By providing native support for 1-bit data formats used for chip-rate processing, TigerSHARC pioneers a new class of software-defined radios and serves applications that were previously the exclusive domain of expensive ASICs (application-specific integrated circuits) and FPGAs (field-programmable gate arrays). And by moving to a software-centric design model, TigerSHARC processors allow IP reuse, which greatly enhances R&D productivity throughout each successive product generation.
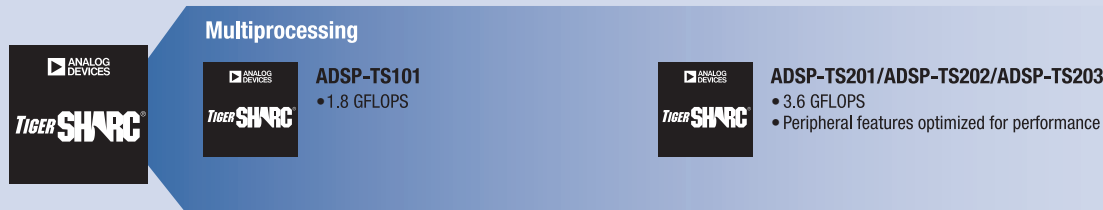
The TigerSHARC processors provide a broad range of price and performance points to meet the needs of many different applications. The ADSp-TS201 is offered at 500 MHz and 600 MHz with 24 Mb of on-chip memory, while the ADSP-TS202 and ADSP-TS203 are offered at 500 MHz with 12 Mb and 4 Mb of on-chip memory, respectively.

Soft Baseband Platform

The TigerSHARC processor supports the massive signal processing and memory demands of communications baseband modem implementations. It is the first general-purpose processor capable of homogeneous, low cost, flexible, and scalable baseband implementations without the use of external ASICs or memory and does not require an internal hardware accelerator.

The TigerSHARC processor is designed specifically to handle all of the demands of a various baseband implementation from a MIPS, memory, and I/O perspective. This enables a compact, homogeneous implementation with a simple control interface that is flexible, scalable, and low cost.

TigerSHARC Processor Product Portfolio

Multiprocessing

ADSP-TS101
• 1.8 GFLOPS

ADSP-TS201/ADSP-TS202/ADSP-TS203
• 3.6 GFLOPS
• Peripheral features optimized for performance

TigerSHARC Processor Family Selection Table

Part Number	Performance		Memory		DMA (Channels)	Peripheral Options			Voltage (V) Nominal		Total Core Power Typ (mW)[1]	Packaging and Temperature Range Options[2,3]		Price @ 1k ($U.S.)[4]	Availability
	Clock Speeds (MHz)	MMACS	On-Chip L1 DRAM (Bits)	External Memory Type Supported		Ports/Features	Number of GPIOs	Timers	Core V_DDINT (Max Speed)	External (I/O)		Package[2,3]	Temperature Range (Non-Automotive Grade)		
ADSP-TS201	500	4000 (16-bit) 1000 (32-bit)	24M	Async, SDRAM	14	4 LVDS link ports, host port, cluster bus (up to 8)	4	2	1.05	2.5, 1.5 DRAM	2163	25 mm × 25 mm, 1.0 mm, 576-ball BGA_ED	−40°C to +105°C −40°C to +85°C	252.25	Production
	600	4800 (16-bit) 1200 (32-bit)							1.20	2.5, 1.6 DRAM	3480		−40°C to +85°C	277.47	
ADSP-TS202	500	4000 (16-bit) 1000 (32-bit)	12M						1.05	2.5, 1.5 DRAM	2163	25 mm × 25 mm, 1.0 mm, 576-ball BGA_ED	−40°C to +85°C	209.51	
ADSP-TS203	500	4000 (16-bit) 1000 (32-bit)	4M		10	2 LVDS link ports, host port, cluster bus (up to 8)			1.05		2163	25 mm × 25 mm, 1.0 mm, 576-ball BGA_ED	−40°C to +85°C	184.49	
ADSP-TS101	250	2000 (16-bit) 500 (32-bit)	6M (SRAM)	Async	14	4 link ports, host port, cluster bus (up to 8)	4	1	1.25	3.3	1500	27 mm × 27 mm, 1.0 mm, 625-ball PBGA; 19 mm × 19 mm, 0.8 mm, 484-ball PBGA	−40°C to +85°C	193.88	Production
	300	2400 (16-bit) 600 (32-bit)	6M (SRAM)						1.25		1875			231.40	

NOTES

[1] Power (mW) stated for maximum core operating speed of the device at T_CASE = 25°C (V_DD nominal, I_DD-TYP supply current). Please refer to associated data sheet and EE notes for further details and complete power calculation information.

[2] All DSP products available in RoHS compliant options. Please refer to data sheet for complete information.

[3] All packaging, operating temperature, and grade combinations may not be available. Please refer to data sheet for full information and contact ADI for options outside those listed.

[4] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

ADSP-TS203 TigerSHARC Processor
500 MHz Processor with 4 Mb On-Chip DRAM

The ADSP-TS203 TigerSHARC processor is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions. The TigerSHARC processor is well-suited to video applications as well as defense, medical imaging, and industrial instrumentation.

The ADSP-TS203 features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC processor to offer unrivaled performance. At a 500 MHz clock rate, the ADSP-TS203 offers the industry's highest 16-bit fixed-point and 32-bit floating-point performance. The ADSP-TS203 has a 32-bit floating-point 1024-point complex FFT time of 18.8 μs and provides 1000 MFLOPS per watt.

ADSP-TS203 Performance

- 500 MHz, 2 ns instruction rate processor core
- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit, fixed-point operations per cycle (3.0 GFLOPS or 12.0 GOPS performance)
- 2-cycle, interlocked execution pipe
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Features

- Static superscalar architecture that supports 1-, 8-, 16-, and 32-bit fixed-point, as well as floating-point, data processing
- High performance 500 MHz, 2 ns instruction rate processor core
- 4 Mb on-chip embedded DRAM internally organized in 6 banks with user-defined partitioning
- 10-channel, zero-overhead DMA controller
- 4 internal 128-bit wide internal buses providing a total memory bandwidth of 32 GBps
- Single-instruction, multiple-data (SIMD) operation supported by 2 computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- 2 LVDS link ports with each operating up to 250 MBps per direction for serial interfacing
- 32-bit cluster bus with operation up to 500 MBps for parallel interfacing
- Assembly and C language programmability
- Core voltage: 1.05 V

Applications

- Video
- Medical imaging
- Industrial and instrumentation
- Military

Part Number	Max (MHz)	On-Chip Memory DRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS203SABP-050	500	4	576-ball PBGA	184.49 to 206.89
ADSP-TS203SABPZ050	500	4	576-ball PBGA	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

A = industrial temperature (–40°C to +85°C case).

Z = RoHS compliant part.

ADSP-TS202 TigerSHARC Processor
500 MHz Processor with 12 Mb On-Chip DRAM

The ADSP-TS202 TigerSHARC processor is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions. The TigerSHARC processor is well-suited to video and communication applications as well as defense, medical imaging, and industrial instrumentation.

The ADSP-TS202 features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC processor to offer unrivaled performance. At a 500 MHz clock rate, the ADSP-TS202 offers the industry's highest 16-bit fixed-point and 32-bit floating-point performance. The ADSP-TS202 has a 32-bit floating-point 1024-point complex FFT time of 18.8 μs and provides 1000 MFLOPS per watt.

ADSP-TS202 Performance

- 500 MHz, 2 ns instruction rate processor core
- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit fixed-point, operations per cycle (3.0 GFLOPS or 12.0 GOPS performance)
- 2-cycle, interlocked execution pipe
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Features

- Static superscalar architecture that supports 1-, 8-, 16-, and 32-bit fixed-point, as well as floating-point, data processing
- High performance, 500 MHz, 2 ns instruction rate processor core
- 12 Mb on-chip embedded DRAM internally organized in 6 banks with user-defined partitioning
- 14-channel, zero-overhead DMA controller
- 4 internal 128-bit wide internal buses, providing a total memory bandwidth of 32.0 GBps
- SIMD operation supported by 2 computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- 4 LVDS link ports with each operating up to 500 MBps per direction for serial interfacing
- Configurable cluster bus (32- or 64-bit) with operation up to 1 GBps for parallel interfacing
- Assembly and C language programmability
- Core voltage: 1.05 V

Applications

- Communications
- Video
- Medical imaging
- Industrial and instrumentation
- Military

Part Number	Max (MHz)	On-Chip Memory DRAM (Mb)	Package	Price @ 1k ($U.S.)[1]
ADSP-TS202SABPZ050	500	12	576-ball PBGA	209.51

NOTES

[1] Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

A = industrial temperature (−40°C to +85°C case).

Z = RoHS compliant part.

ADSP-TS201 TigerSHARC Processor
600 MHz Processor with 24 Mb On-Chip DRAM

The ADSP-TS201 is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions. The TigerSHARC processor is well-suited to video and communication markets, including the 3G cellular and broadband wireless base stations, as well as defense, medical imaging, and industrial instrumentation.

The ADSP-TS201 features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC processor to offer unrivaled performance. At a 600 MHz clock rate, the ADSP-TS201 offers the industry's highest 16-bit fixed-point and 32-bit floating-point performance. The ADSP-TS201 has a 32-bit floating-point 1024-point complex FFT time of 15.7 μs and provides 1000 MFLOPS per watt.

ADSP-TS201 Performance

- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit fixed-point, operations per cycle (3.6 GFLOPS or 14.4 GOPS)
- 2-cycle, interlocked execution pipe
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Applications

- Wireless infrastructure
- Performance driven embedded applications
  - Military hardware
  - Medical equipment
  - Industrial and instrumentation
  - Software-defined radios

Features

- Static superscalar architecture that supports 1-, 8-, 16-, and 32-bit fixed-point, as well as floating-point, data processing
- High performance, 600 MHz, 1.67 ns instruction rate processor core
- 24 Mb on-chip embedded DRAM internally organized in 6 banks with user-defined partitioning
- 14-channel, zero-overhead DMA controller
- Enhanced communications instruction set for wireless infrastructure applications allows for the TigerSHARC processor to offer complete baseband processing
- 4 internal 128-bit wide internal buses, providing a total memory bandwidth of 38.4 GBps
- Software radio approach allows the adoption of a single platform for multiple wireless telecommunication standards
- SIMD operation supported by 2 computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- 4 LVDS link ports with each operating up to 500 MBps per direction for serial interfacing
- Configurable cluster bus (32- or 64-bit) with operation up to 1 GBps for parallel interfacing
- Assembly and C language programmability
- Core voltage: 1.05 V (500 MHz) or 1.2 V (600 MHz)

ADSP-TS201 Block Diagram
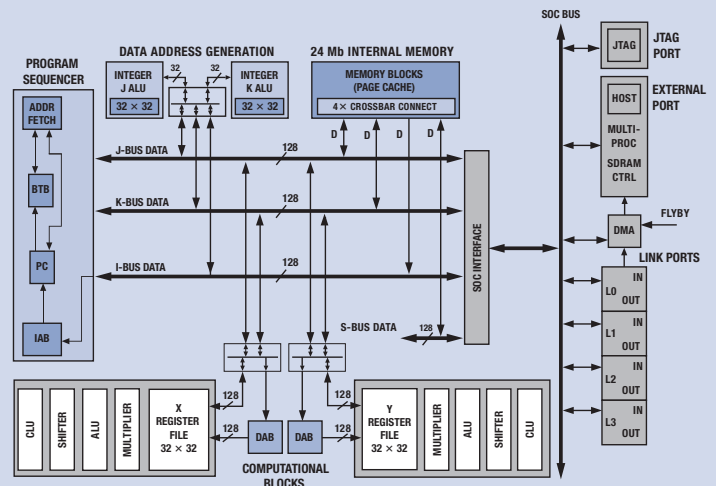
Part Number	Max (MHz)	On-Chip Memory DRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS201SABP-050	500	24	576-ball PBGA	
ADSP-TS201SABP-060	600	24	576-ball PBGA	
ADSP-TS201SABPZ050	500	24	576-ball PBGA	
ADSP-TS201SABPZ060	600	24	576-ball PBGA	252.25 to 339.43
ADSP-TS201SYBP-050	500	24	576-ball PBGA	
ADSP-TS201SYBPZ050	500	24	576-ball PBGA	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

A = industrial temperature (–40°C to +85°C case).

Y = automotive temperature (–40°C to +105°C case).

Z = RoHS compliant part.

ADSP-TS101 TigerSHARC Processor
300 MHz Processor with 6 Mb On-Chip SRAM

The ADSP-TS101 is the first member of the TigerSHARC processor family. It is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions.

The ADSP-TS101 features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC processor to offer unrivaled performance. At a 300 MHz clock rate, the ADSP-TS101 offers the 16-bit fixed-point performance and a 32-bit floating-point 1024-point complex FFT time of 32.5 μs and 1000 MFLOPS per watt.

ADSP-TS101 Performance

- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit, fixed-point operations per cycle (1800 MFLOPS or 7.2 GOPS performance)
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Applications

- Wireless infrastructure
- Medical, CT, ultrasound
- Sonar and radar systems
- Flight simulators
- Infrastructure equipment
- Military smart munitions
- Test equipment
- Imaging, printers
- Wireless broadband access
- Industrial applications

Features

- Static superscalar architecture supports 1-, 8-, 16-, and 32-bit fixed-point, as well as floating-point, data processing
- SIMD operation supported by two computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- Assembly and C language programmability
- Up to 300 MHz, 3.3 ns instruction rate processor core
- 6 Mb on-chip SRAM internally organized in 3 banks with user-defined partitioning
- 14-channel, zero-overhead DMA controller
- 4 LVTLL link ports operating up to 250 MBps for serial interfacing
- Configurable cluster bus (32- or 64-bit) with operation up to 800 MBps for parallel interfacing
- Enhanced communications instruction set for wireless infrastructure applications for complete baseband processing
- 3 internal 128-bit wide internal buses, providing a total memory bandwidth of 14.4 GBps
- Software radio approach allows for the adoption of a single platform for multiple wireless telecommunication standards
- Core voltage: 1.2 V

Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS101SAB1-000	250	6	625-ball PBGA	
ADSP-TS101SAB1-100	300	6	625-ball PBGA	
ADSP-TS101SAB1Z000	250	6	625-ball PBGA	
ADSP-TS101SAB1Z100	300	6	625-ball PBGA	
ADSP-TS101SAB2-000	250	6	484-ball PBGA	193.88 to 259.49
ADSP-TS101SAB2-100	300	6	484-ball PBGA	
ADSP-TS101SAB2Z000	250	6	484-ball PBGA	
ADSP-TS101SAB2Z100	300	6	484-ball PBGA	

NOTES
[1]Prices are quoted in U.S. dollars and represent year 2011 suggested resale pricing. All prices are budgetary and subject to change. Customers are advised to obtain the most current and complete pricing information from ADI prior to placing orders. Prices shown indicate a price range and will vary depending on speed, package type, and/or temperature range and grade.

A = industrial temperature (–40°C to +85°C case).

Z = RoHS compliant part.

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