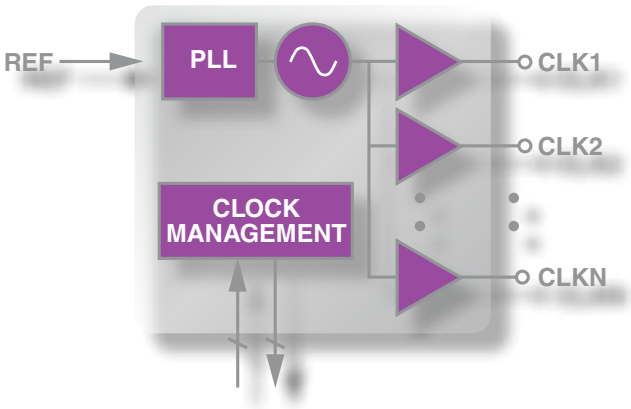
Clock & Timing IC Solutions

www.hittite.com



Hittite has developed an industry-leading line of high performance clock distribution and clock generation products that enable the system designer to maximize the performance from data converters and physical layer (PHY) components.

Hittite
MICROWAVE PRODUCTS
FROM ANALOG DEVICES

Analog, Digital & Mixed-Signal ICs,
Modules, Subsystems & Instrumentation, DC - 110 GHz

REF# CT-0313

CORE COMPETENCIES

Hittite Core Competencies in Clock & Timing ICs:

Clock Generation

- *Programmable Output Frequencies for Flexible Frequency Planning*
- *Industry Leading Phase Jitter of <80 fs RMS*
- *Advanced Phase Noise Spur Reduction Technique to Reduce Noise Sensitivity*

Clock Management

- *Jitter Attenuation of Backplane Clocks Up to 3 GHz*
- *Fractional-N Frequency Generation Using Proprietary Delta-Sigma Modulation Technique*
- *Exact Frequency Mode to Generate Clocks with 0 Hz Error*

Clock Distribution

- *Clock Trees with Negligible Additive Jitter & Low Propagation Delays*
- *Best-in-Class Phase Noise Floor of <-165 dBc/Hz*
- *Clock De-Skew & Delay Management*

Across All Markets:

Our SMT packaged clock generators operate up to 3 GHz, and are ideal for a wide range of high performance cellular/4G infrastructure, fiber optic and networking applications, and deliver best-in-class jitter and industry-leading phase noise floor. Hittite's configurable Clock & Timing ICs offer flexibility in frequency planning and system design. In communications applications, low jitter clock ICs improve link Bit Error Rate (BER) and eye diagram performance for higher bandwidth communication interfaces. In control applications, Hittite's proprietary Fractional-N clock generation architecture allows for configurable frequencies. Similarly, in sensors and entertainment applications, clock generation and distribution devices facilitate clock trees that support multiple frequencies to address system-wide synchronization challenges.

Hittite Heritage:

Hittite has broad engineering expertise in high frequency PLL, VCO and signal amplifiers. As bandwidth requirements increase, the clock speeds that are required to synchronize data converters and PHY components increase as well. Hittite's focus on innovation in high frequency building blocks enable the industry leading Clock & Timing IC products that meet the demands of next generation designs.

CLOCK & TIMING ICs

Clock Distribution

	Max. Clock Rate (GHz)	Function	Input	Output	Phase Jitter (12 k to 20 MHz)	Rise/Fall Time (ps)	Channel Skew (ps)	Disable Mode	Power Supply (V)	Package	ECCN Code	Part Number
NEW!	4	Clock Divider & Delay Management	LVPECL, LVDS, CML, CMOS	LVPECL	13 fs RMS	90	300 to 1500	Yes	5 or 3.3	LP3	3A001.a.11.b	HMC988LP3E
	8	1:9 Fanout Buffer	LVPECL, LVDS, CML, CMOS	LVPECL	8 fs RMS	65	3.1	Yes	3.3	LP5	3A001.a.11.b	HMC987LP5E

Clock Generators

	Max. Frequency (MHz)	Function	Typical Phase Jitter (fsRMS)	Phase Noise Floor (dBc/Hz)	Maximum Reference Freq. (MHz)	Typical Power Consumption (W)	Figure of Merit (Frac/Int) (dBc/Hz)	Package	ECCN Code	Part Number
NEW!	500	Integer Mode PLL (x1, x5, x10)	Defined by VCXO	Defined by VCXO	140	0.0064	-208	MS8	EAR99	HMC1031MS8E
	350	Clock Generator with Fractional-N PLL+VCO	116 / 75	-165	350	0.86	-227 / -230	LP6G	3A001.a.11.b	HMC1032LP6GE
NEW!	550	High Performance +3.3 V Clock Generator	99	-163	350	0.64	-226 / -227	LP6G	3A001.a.11.b	HMC1033LP6GE
NEW!	2500	High Performance +3.3 V Clock Generator	97	-163	350	0.57	-226 / -227	LP6G	3A001.a.11.b	HMC1035LP6GE
	3000	Clock Generator with Fractional-N PLL+VCO	118 / 78	-165	350	0.86	-227 / -230	LP6G	3A001.a.11.b	HMC1034LP6GE

Hittite Clock & Timing ICs

Hittite Clock & Timing ICs offer excellent Power Supply Rejection Ratios (PSRR) and spur reduction. For demanding applications where additional supply noise filtering and regulation is required, low noise linear voltage regulators from Hittite reduce system complexity and offer excellent power supply noise immunity. These industry leading regulators are assembled in space saving LP3 (3 mm x 3 mm) packages and offer noise spectral densities of <7 nv/sqrt (Hz) at 1 kHz offsets.

DC POWER CONDITIONING - Linear Voltage Regulators

Input Voltage (V)	Function	Output Voltage (V)	Output Current (mA)	Power Supply Rejection Ratio (PSRR) (dB)		Output Noise Spectral Density (nV/√Hz)		Regulated Outputs	Package	ECCN Code	Part Number
				1 kHz	1 MHz	1 kHz	10 kHz				
3.35 - 5.6	Quad High PSRR	2.5 - 5.2	15 - 100	80	60	7	3	4	LP3	EAR99	HMC860LP3E
3.35 - 5.6	Low Noise, High PSRR	1.8 - 5.2	500	80	60	7	3	4	LP3	EAR99	HMC1060LP3E
4.8 to 5.6	Low Noise, High PSRR	1.8 to 5.1	400	60	30	6	3	1	LP3	EAR99	HMC976LP3E

Hittite's website contains full datasheets, application notes, as well as ordering information for our complete product offering of over 1075 products across 36 product lines.

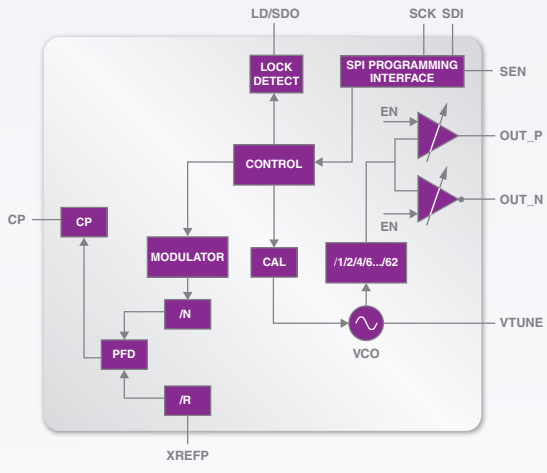
HMC1033LP6GE & HMC1035LP6GE

3.3V High Performance Programmable Clock Generator, 25 to 2500 MHz

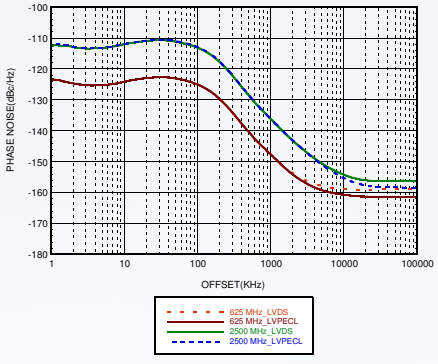
NEW!

40-Lead, 6 x 6 mm SMT Package

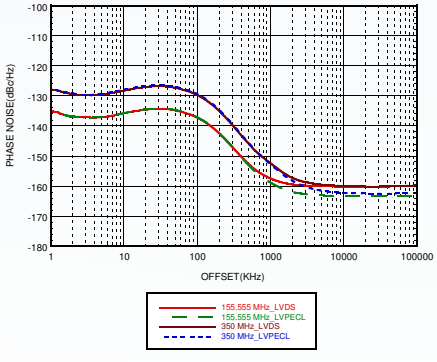
- *Integer & Fractional-N Mode Frequency Translation from 25 MHz to 2.5 GHz*
- *Configurable Outputs: LVDS-Compatible or LVPECL with 12 Settings to Adjust the Signal Amplitude*
- *"Phase Noise on Demand" feature to switch between "Power Priority" and "Performance Priority" Modes*
- *Adjustable PLL Loop Bandwidth via External Loop Filter to Control Setting Time & Noise Profile*
- *Output Disable/Mute Control*
- *Lock Detect Signal*
- *Exact Frequency Mode to Achieve Reference Frequency Tuning for DDS Replacement Applications*



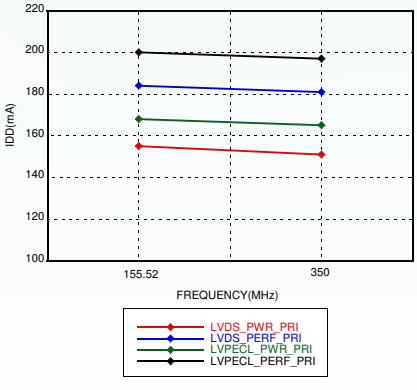
HMC1035LP6GE - Excellent Noise Floor Improves Data Converter SNR



HMC1033LP6GE - Superior PN Performance Improves PHY BER & Link Jitter



HMC1033LP6GE - Power Savings with Phase Noise on Demand Feature



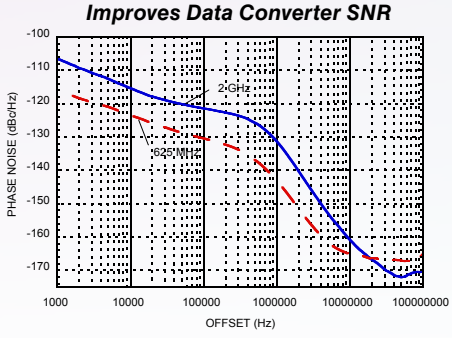
HMC1032LP6GE & HMC1034LP6GE

Clock Generator with Fractional-N PLL & Integrated VCO, 125 to 3000 MHz

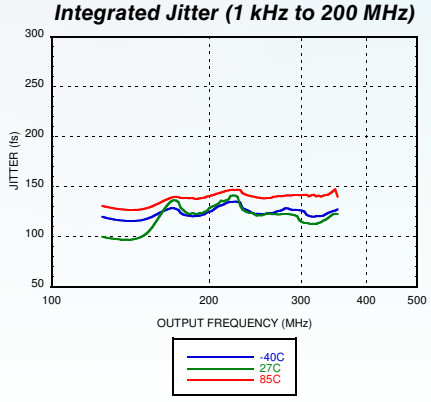
40-Lead, 6 x 6 mm SMT Package

- *125 MHz to 3000 MHz (HMC1034LP6GE)*
- *125 MHz to 350 MHz (HMC1033LP6GE)*
- *<80 fs Phase Jitter @ 2 GHz (12k to 20 MHz Integration), -170 dBc/Hz Phase Noise Floor*
- *24-Bit Delta-Sigma Fractional-N Synthesis achieves <3 Hz Typical Resolution*
- *Adjustable Drive Strength, CML True Differential Outputs*
- *Adjustable Loop Bandwidth via External Loop Filter (2nd Order R-C)*

Excellent Phase Noise Improves Data Converter SNR



Fractional-N Mode Integrated Jitter (1 kHz to 200 MHz)



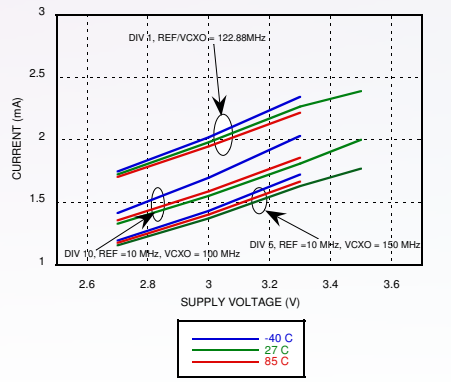
HMC1031MS8E

Clock Generator with Integer-N PLL, 0.1 to 500 MHz

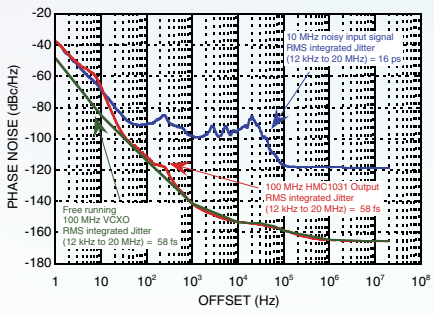
8-Lead, 4.8 x 3.0 mm SMT Package

- *Integer-N PLL Clock Generator with External VCO/VCXO*
- *Ultra-Low Power Consumption: <2 mA Typical in Normal Operation*
- *Hardware Pin Programmable Reference Clock Multiplication Ratios of x1, x5, x10*
- *Phase Noise Floor (Figure of Merit): -208 dBc/Hz (Typical)*

Very Low Power Consumption



Typical Closed Loop Phase Noise, as Jitter Attenuator

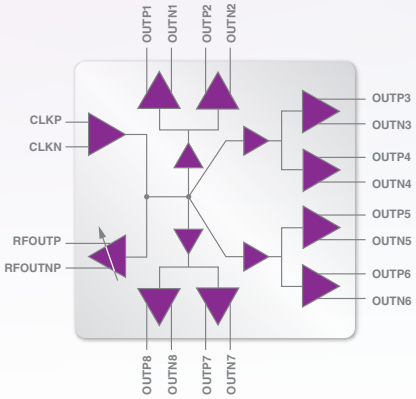


HMC987LP5E

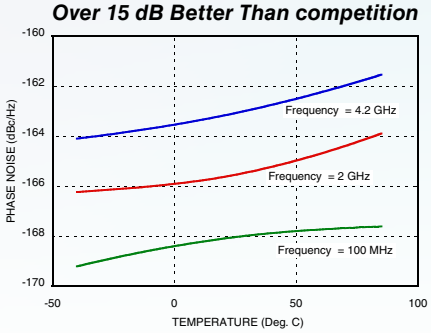
3.3V Low Noise, 1:9 Fanout Buffer, DC to 8 GHz

32-Lead, 5 x 5 mm
SMT Package: 25 mm²

- 8 LVPECL Outputs (800 mVp-p into 50 Ohm Single-Ended Load)
- 1 Adjustable Power RF Output (-3 to 6 dBm)
- Flexible Input Buffer: LVPECL or AC-Coupled Input Compatible
- Serial or Parallel Control & Pin-Controlled Chip Enable
- Single-Ended or Differential-to-Differential Conversion
- Optimized for Very Low Output-to-Output Skew



-166 dBc/Hz Phase Noise Floor is Over 15 dB Better Than competition

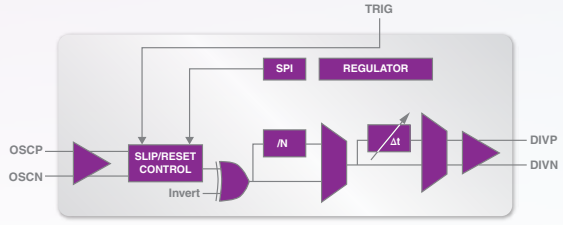


HMC988LP3E

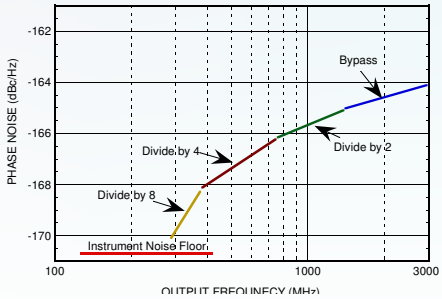
3.3V Programmable Digital Delay & Divider IC, DC to 4 GHz

16-Lead, 3 x 3 mm
Leadless QFN Package

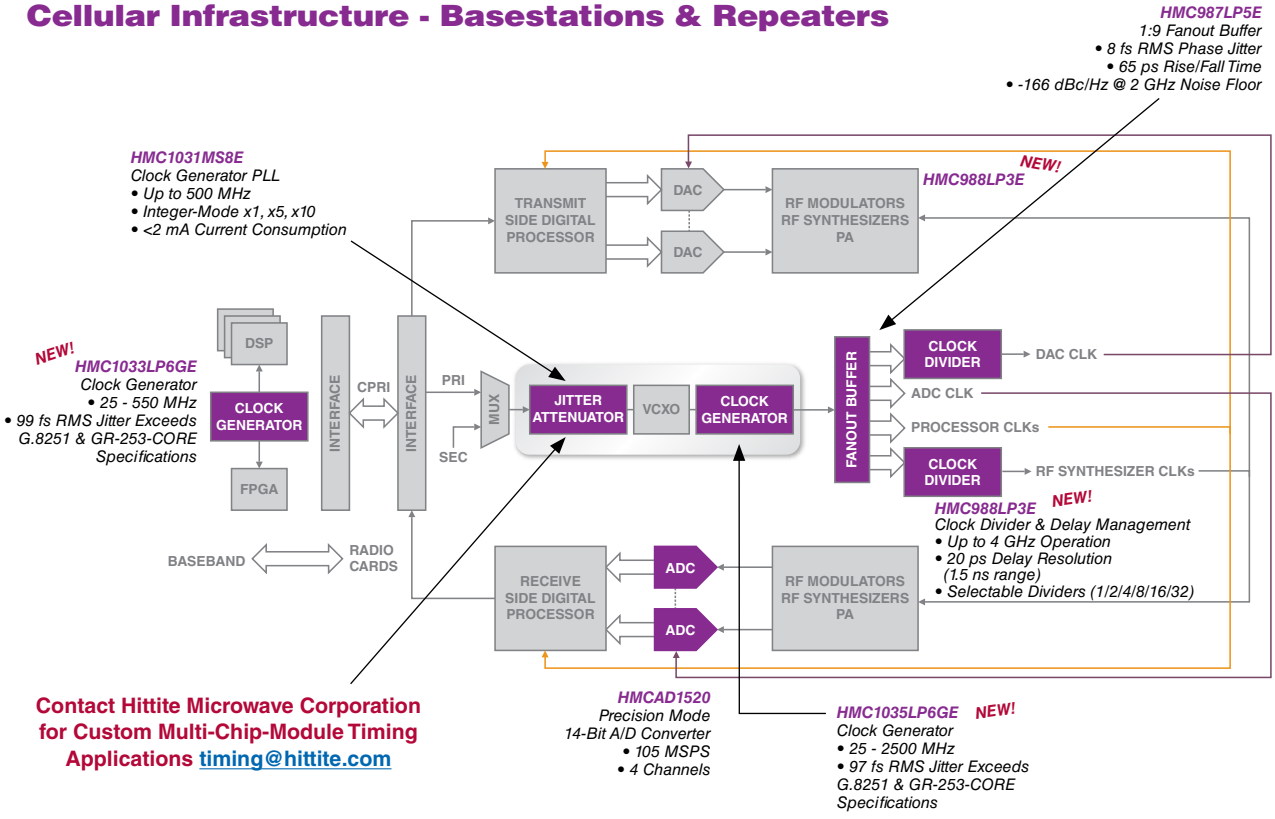
- Single Channel Clock Divider & Delay Management IC
- Programmable Clock Divider by 1/2/4/8/16/32
- Delay Adjustment in 1/2 Clock Cycles or in 60 Steps of 20 ps
- -170 dBc/Hz Phase Noise Floor for Negligible Jitter Contribution
- 800 mVp-p LVPECL Output
- 3.3V Operation (or 5V with Optional On-Chip Regulator)



Ideal for Data Converter Sample Clock Phase Adjustment with Excellent Phase Noise Floor



Cellular Infrastructure - Basestations & Repeaters



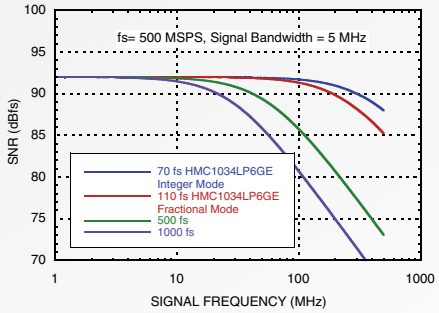
Data Converter Clocking with Hittite Clock Generators

Selecting the right components for clock generation and data conversion enables a designer to extract the best performance from a given architecture. Data converter dynamic range and linearity performance can be improved by careful consideration of clock generator characteristics.

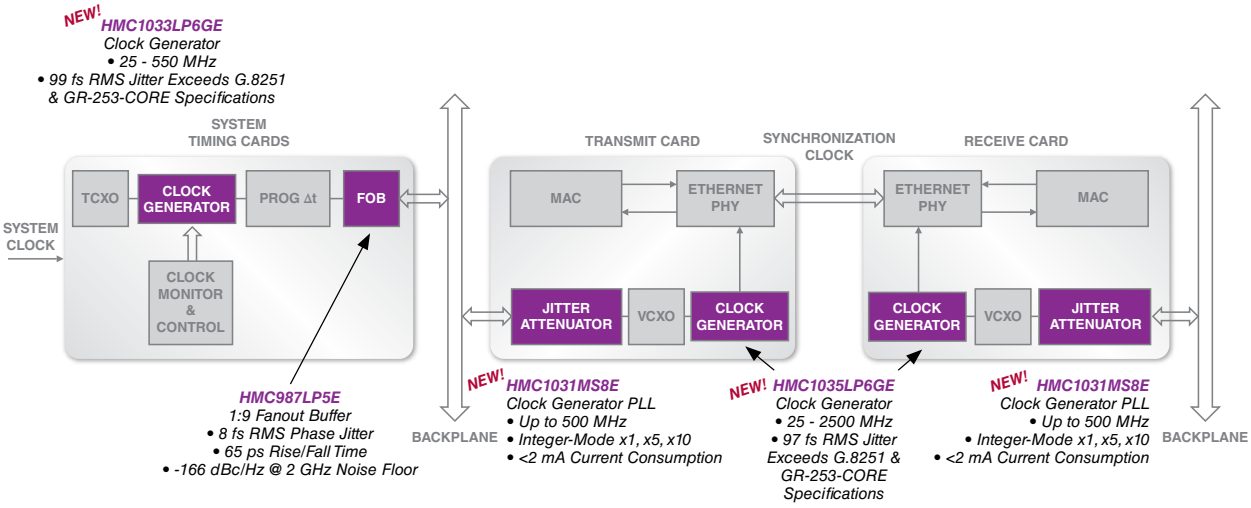
Important criteria to consider when choosing a clock generator are phase jitter and phase noise floor, which impact the SNR of the data converter being clocked. As the graph below indicates, the low phase noise floor of the chosen clock generator as well as its low integrated phase jitter helps to minimize the SNR degradation at higher ADC/DAC frequencies in multi-acquisition applications. The HMC1034LP6GE with integer-mode configuration offers the lowest clock jitter and offers significant improvements over clock generators with higher jitter.

Hittite's Clock & Timing ICs are designed with data converter applications in mind, and work well with Hittite's high speed ADC devices. Our clock generators with industry's best close-in and far-from-carrier phase noise are ideally suited to extract the best performance from data converters.

ADC SNR vs. Clock Jitter and Input Frequency



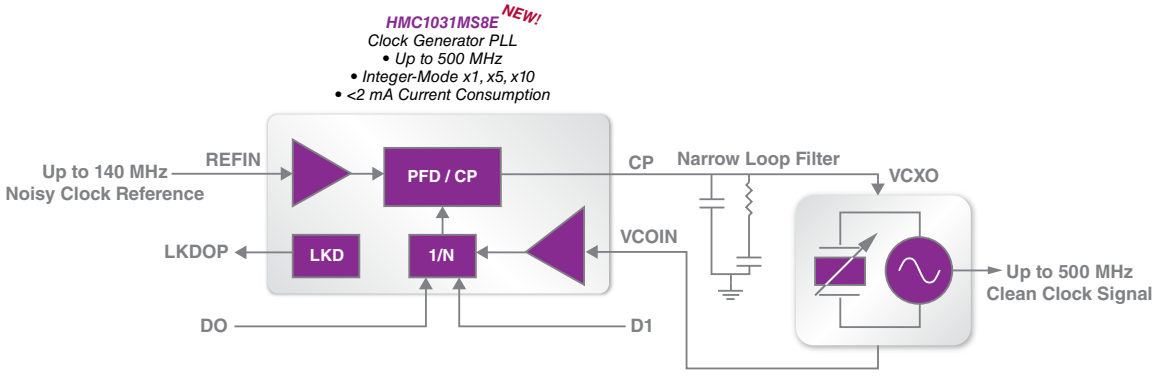
10G/40G/100G Networking & Storage Line Cards



Frequency Translation with HMC1031MS8E

Together with an external loop filter and a Voltage Controlled Crystal Oscillator (VCXO), the HMC1031MS8E forms a complete clock generator solution targeted at low frequency jitter-cleaner and reference clock generation applications. Quite often, the reference clock in a test & measurement or a communications system is a high accuracy Oven Controlled Crystal Oscillator (OCXO) with excellent long-term stability.

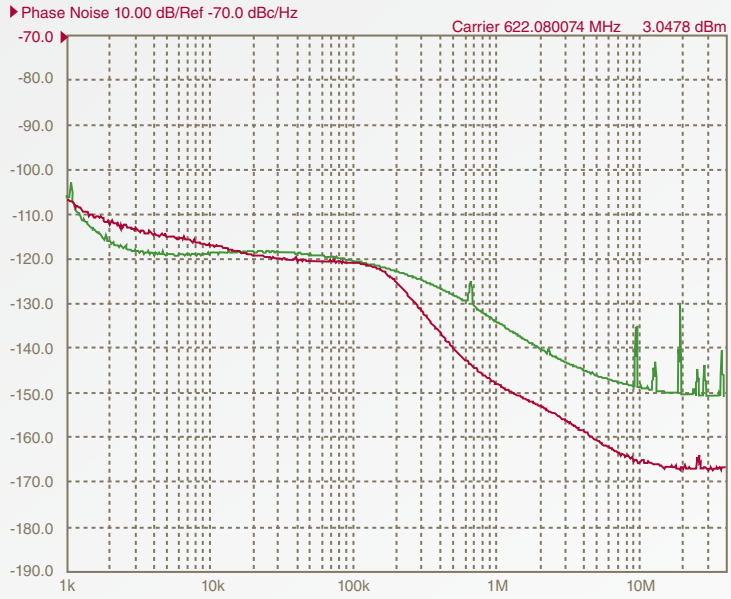
The HMC1031MS8E may find applications when the OCXO frequency needs to be multiplied up to a higher rate to drive the primary clock inputs in a system. The device offers a very low power, small package and high performance method to multiply its incoming frequency in x1, x5 and x10 rates. Such multiplication is needed because the higher reference clocks improve phase noise, ADC/DAC SNR, clock generator jitter and PHY BERs. In this scheme, the HMC1031MS8E may be connected to an external low cost VCXO (e.g. at 50 MHz or 100 MHz), and lock this external VCXO to the excellent long-term stability of the OCXO.



Clock Generation

Our Clock & Timing solutions are ideal for communications, control, sensing & entertainment electronic systems across all markets. Hittite Clock Generation ICs enable deterministic system design with low noise clock signals that have very low jitter and fast rise and fall times.

HMC1034LP6GE vs. Competitor



Competitor

- -150 dBc/Hz Phase Noise Floor
- 228 fs Jitter Generation, 12 k to 20 MHz
- 500 ps Rise and Fall Time

Hittite

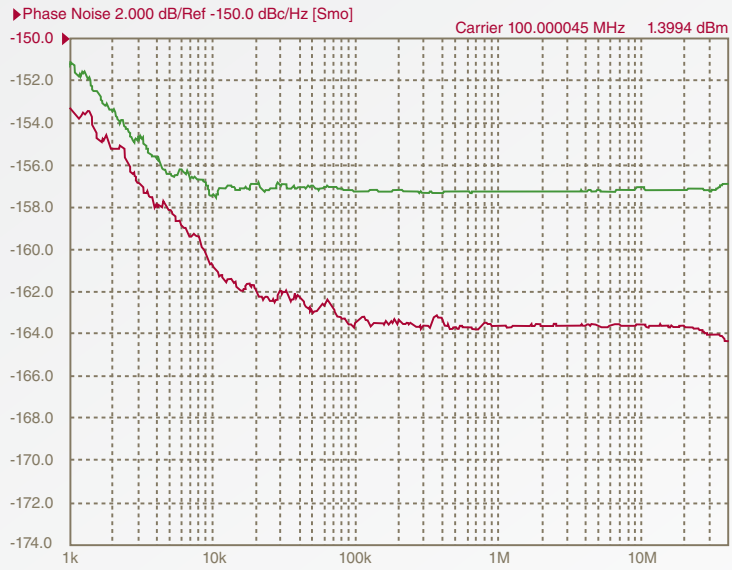
- -166 dBc/Hz Phase Noise Floor
- 99 fs Jitter Generation, 12 k to 20 MHz
- 125 ps Rise and Fall Time

16 dB Lower Phase Noise Floor & Faster Rise and Fall Time = Better System Performance

Clock Distribution

Hittite Clock Distribution ICs with the industry's best phase noise floor performance are used to distribute Data Converter Sample Clocks with negligible additive jitter.

HMC987LP5E vs. Competitor



Competitor

- -157 dBc/Hz Phase Noise Floor
- 102 fs Jitter Generation, 12 k to 20 MHz
- 130 ps Rise and Fall Time

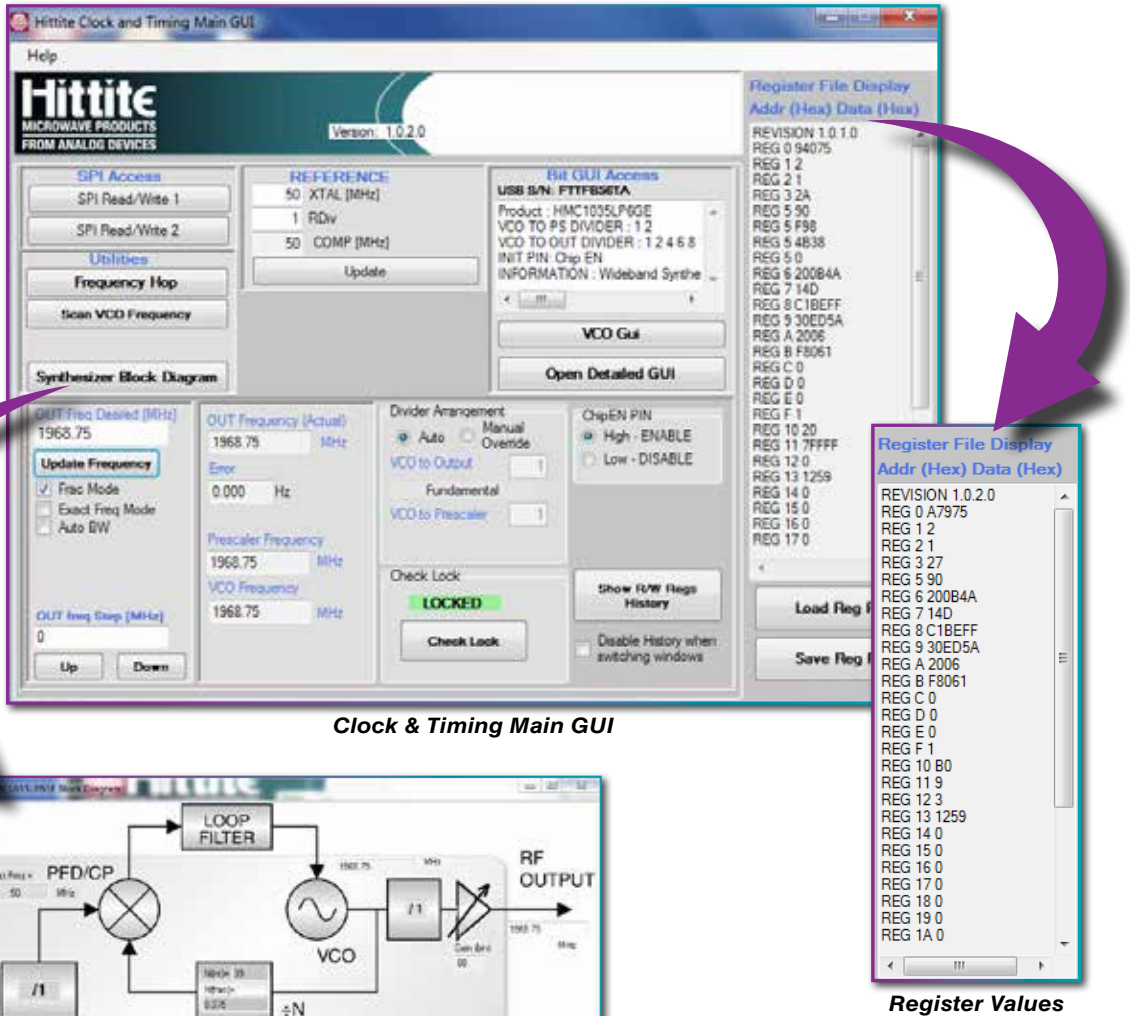
Hittite

- -164 dBc/Hz Phase Noise Floor
- 59 fs Jitter Generation, 12 k to 20 MHz
- 65 ps Rise and Fall Time

7 dB Lower Phase Noise Floor & Faster Rise and Fall Time = Better System Performance

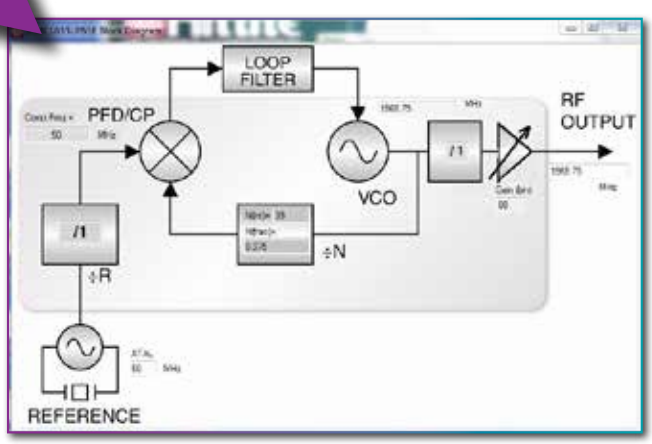
CLOCK & TIMING EVALUATION KIT

Hittite's Clock & Timing Evaluation Software enables users to communicate with, and control, Hittite Clock & Timing ICs with their PCs via the provided USB connection board. The software features a simple GUI to set reference and output frequencies, program registers, and select operation modes.



Clock & Timing Main GUI

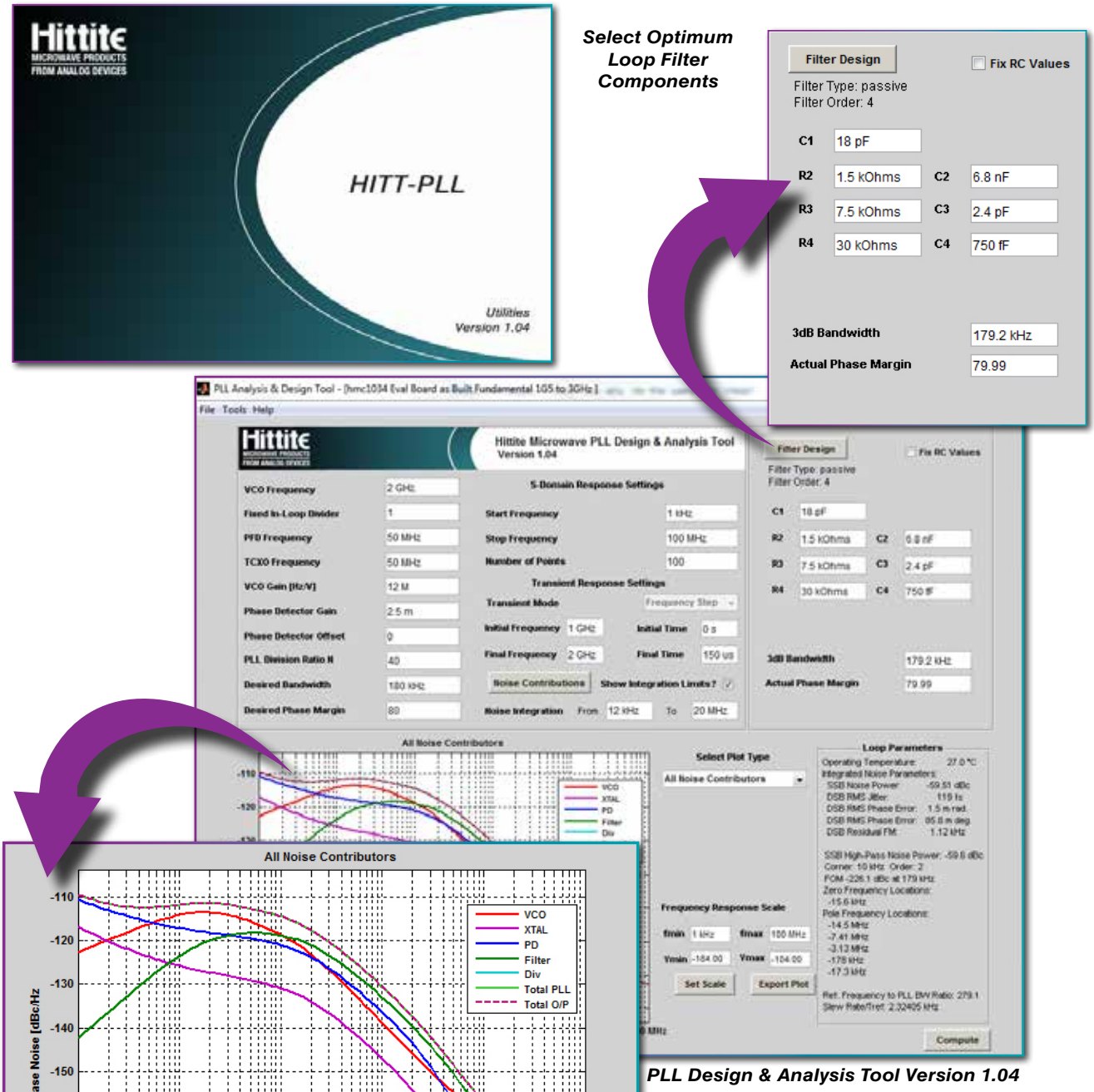
Register Values



Synthesizer Block Diagram

HITT-PLL: Hittite's Clock Design & Analysis Tool

- Accurately Simulate Your Design
- Easily Optimize Performance by Varying Loop Filter Components and Noise Profiles
- Reduce Design Time by Generating Phase Noise Plots and Jitter Measurements
- Model Transient Behavior to Estimate Loop Settling Times and Frequency Changes



PLL Design & Analysis Tool Version 1.04

Programmed Noise Sources Can be Modified by Individual Sources

CLOCK & TIMING IC SOLUTIONS

Contact Us: timing@hittite.com

Hittite Microwave Corporate Headquarters & Sales Office Locations

Hittite Microwave Corporation

Corporate Headquarters

2 Elizabeth Drive
Chelmsford, MA 01824
USA
Tel: 978-250-3343
Fax: 978-250-3373
Email: sales@hittite.com

Hittite Microwave International Ltd.

International Operations

Cork Airport Business Park, Bldg 6900
Kinsale Road
Cork, Ireland
Tel: +353 21 240 7669
Fax: +353 21 240 7997
Email: sales@hittite.com

Hittite Worldwide Sales Offices

Americas

Eastern - North America
Boston, MA
Phone: 978-270-3167
usa-east-north@hittite.com

Vienna, VA
Phone: 312-485-8730
usa-east-south@hittite.com

Central (North) - North America
Chicago, IL
Phone: 312-485-8730
usa-north@hittite.com

Central (South) - North America
Dallas, TX
Phone: 817-727-7146
usa-south@hittite.com

West (South)
Los Angeles, CA
Phone: 626-961-5602
usa-west@hittite.com

West (North)
San Jose, CA
Phone: 978-518-1792
usa-west-north@hittite.com

Europe, Middle East & Africa

United Kingdom, Ireland, Spain, Portugal, Greece & Turkey
Hittite Microwave Europe Limited
Phone: +44-7811-267418
Fax: +978-250-3373
europe@hittite.com

France, Italy & Benelux
Hittite Microwave Deutschland GmbH
Phone: +44-7811-267418
Fax: +978-250-3373
germany@hittite.com

Denmark, Finland, Norway & Sweden
Hittite Microwave Nordic AB
Phone: +46-761-763969
nordic@hittite.com

Finland Office
Phone: +46-761-763969
Fax: +46-8-752-9900

Central & Eastern Europe
Hittite Microwave Deutschland GmbH
Phone: +49-8031-97654
Fax: +49-8031-98883
germany@hittite.com

Asia & Pacific

Australia & New Zealand
Hittite Microwave Corporation
Phone: 978-250-3343
Fax: 978-250-3373
ausnz@hittite.com

India
Hittite Microwave India Pvt. Ltd.
Phone: +91-40-44311254
Fax: +91-40-44311100
india@hittite.com

Japan
Hittite KK
Phone: +81-3-5652-5772
Fax: +81-3-5652-6694
japan@hittite.com

Republic of Korea
Hittite Microwave Asia Co., Limited
Phone: +82-2559-0638
Fax: +82-2559-0639
korea@hittite.com

Peoples Republic of China
Hittite Microwave Co., Limited
Shanghai Office
Phone: +86-21-6209-8809
Fax: +86-21-6209-6730
china@hittite.com

Shenzhen Office
Phone: +86-755-3322-2116
Fax: +86-755-3322-2117
shenzhen@hittite.com

Beijing Office
Phone: +86-10-6485 9219
Fax: +86-10-6485 0377
beijing@hittite.com

Xi'an Office
Phone: +86-29-8885-7651
Fax: +86-29-8450-3797
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